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Modular Architecture For Ultra Low Power Switched-Capacitor DC-DC Converters

Author:
Ing.Pablo Castro Lisboa
pcastro@fing.edu.uy

Academic Director:
Prof.Fernando Silveira

Thesis Advisors:
Prof.Fernando Silveira
Prof.Adj.Gabriel Eirea

Montevideo, Uruguay

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Director académico y Co-tutor de tesis:

Prof.Fernando Silveira: _____

Co-Tutor de Tesis:

Prof.Adj.Gabriel Eirea: _____

Tribunal Examinador:

Prof.José Luis Huertas: _____

Prof.Cesar Briozzo: _____

Prof.Agr.Conrado Rossi: _____

A mis padres....
Que me dieron lo más importante.

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Resumen

Este trabajo presenta una arquitectura novedosa para la implementación de convertidores DC-DC de condensadores conmutados de Ultra Bajo Consumo para aplicaciones como dispositivos implantables, redes de sensores inalámbricos, dispositivos portátiles, entre otros. El objetivo es suministrar energía a circuitos digitales tales como microcontroladores usando la técnica the escalado dinámico de voltaje que permite manejar el compromiso entre la performance y el consumo del circuito. Otra importante aplicación de este tipo de convertidores es para las nuevas tecnologías donde los transistores no soportan el voltaje entregado por los distintos tipos de pilas.

Cuantos más niveles de conversión tenga el convertidor mejor se puede aplicar la técnica de escalado dinámico de voltaje. Esto es porque diferentes niveles de performance de un circuito digital necesitan diferentes voltajes de alimentación para minimizar la potencia disipada alcanzando la performance necesaria. Existen algunos trabajos en el área, todos ellos tienen la particularidad de utilizar arquitecturas rígidas basadas en configuraciones particulares para cada nivel de conversión. Esto hace que este tipo de convertidores no sea apropiado para aumentar fácilmente la cantidad de niveles de conversión. La arquitectura propuesta en este trabajo tiene la particularidad de ser modular y permite fácilmente agregar más niveles de conversión si fuera necesario, a la vez que simplifica el diseño

Cada módulo esta compuesto por un condensador y una configuración de cuatro switches. El número de módulos usado en el convertidor define el número de niveles de conversión. Los módulos son conectados en forma de anillo el cual puede ser abierto en cualquiera de los nodos con el fin de conectar la fuente de alimentación. Luego la carga es conectada a uno de los nodos intermedios del anillo según el nivel de conversión deseado.

Dada la modularidad del convertidor un modelo numérico general fue desarrollado. Este modelo permite tener una predicción de la performance del convertidor para un número arbitrario de niveles de conversión. Dado que el modelo utiliza datos extraídos de simulaciones eléctricas y algunos parámetros de la tecnología, fácilmente puede ser usado para cualquier tecnología. El modelo es apropiado para realizar exploraciones del espacio de diseño y evitar los prolongados tiempos de las simulaciones eléctricas.

Un convertidor de cuatro niveles de conversion fue desarrollado y simulado a nivel eléctrico en la tecnología On Semi $0{,}5\mu m$ con un voltaje de alimentación de $2{,}8V$. El pico de eficiencia alcanzado es de $78\,\%$. Esta performance es similar a la alcanzada por los trabajos existentes en la literatura. Para este convertidor la lógica fue implementado, pero no el lazo de control que fija la tensión de salida.

Una novedosa técnica para disminuir las pérdidas en las capacidades parásitas fue propuesta y simulada. Dicha técnica realiza una redistribución de la carga entre las capacidades parásitas que necesitan perder energía y aquellas que necesitan ganarla. Dado que las pérdidas en las capacidades parásitas son dominantes en esta arquitectura, una mejora significativa fue lograda en la eficiencia a partir de la aplicación de esta técnica.

Abstract

This work presents a novel architecture for a step down **Switched Capacitor Converter** for **Ultra Low Power** applications such as implantable devices, Wireless Sensor Nodes, portable devices, etc. The objective is to supply energy to digital circuits such as micro-controllers using the **Dynamic Voltage Scaling** technique that allows to optimize the trade-off between performance and consumption. Other important applications of this type of converters are the newest technologies where the transistors are not able to tolerate the voltage provided by the different types of batteries.

The more conversion ratios the converter has the better to apply the **Dynamic Voltage Scaling** technique it is. This is because different performance levels in digital circuits need different supply voltages to minimize the power consumption while achieving the needed performance. In the literature there are some works in the area, all of them with the particularity of having a rigid architecture based on particular configurations for each conversion level. This makes this type of converters not suitable for adding easily more conversion ratios. The architecture proposed in this work has the particularity of being modular and being able to easily add new conversion ratios if necessary.

Each module (named **Basic Capacitor Cell**) is composed by a capacitor and a four-switch configuration. The number of modules used in the converter defines the number of conversion ratios. The **Basic Capacitor Cells** are connected in a ring configuration that can be opened in each node to connect the supply voltage. Then the load is connected to one of the intermediate nodes.

Given the modularity of the converter a general numerical model was developed. This model allows to predict the performance of the converter for an arbitrary number of conversion ratios. As the model uses some data extracted from electrical simulation and some parameters of the technology, it can easily be used for any technology. The model is suitable to make design space exploration and avoid long electrical simulations times.

A four-conversion-ratios converter was developed and electrically simulated in the technology On Semi $0{,}5\mu m$ with an input voltage of $2{,}8V$. The peak efficiency achieved is $78\,\%$. This performance is similar to the one achieved by existing works in the literature. The logic was implemented but not the control loop.

A novel technique to improve the losses in parasitic capacitances was proposed and simulated. This technique makes a redistribution of the charge between the parasitic capacitances that need to lose energy and those that need to gain energy. Since parasitic capacitances losses are dominant in this architecture a significant efficiency improvement was achieved using this technique.

Index Terms - Ultra Low Power , **Switched Capacitor Converter** , **Dynamic Voltage Scaling** , **Power Management**, **DC-DC Converter** .

CHAPTER 1

Introduction

1.1. Motivation

The increasing emergence of battery-powered devices (notebooks, cell-phones, Wireless Sensor Networks, implantable devices, etc) has increased the efforts to optimize the consumption of these devices and thus increase battery life. This issue in implantable devices is critical because changing the battery involves surgery. The power consumption optimization effort is made at all levels: architecture, low level design, high level design, etc.

Since power consumption in digital circuits is proportional to the square of supply voltage (Equation 1.1[1]) [1], decreasing it is a key factor for the purpose of maximizing battery life. Decreasing the supply voltage has a negative impact in the maximum frequency tolerated by digital circuits. So it is necessary to manage this trade-off decreasing the supply voltage when the performance of the digital circuit becomes lower to save energy and increasing it when the circuit needs a higher performance. This technique is named **Dynamic Voltage Scaling** [2].

$$P_{Digital} = f.C_L.V_{DD}^2 \tag{1.1}$$

On the other hand, the advance of technology has decreased the maximum voltage tolerated by **Integrated Circuits** , even below the voltage provided by different types of batteries (Ni-Cd, Li-ion, etc). So it is clear that having the capability of delivering to digital circuits a supply voltage lower than the provided by batteries is essential. This must be made with efficiency to avoid that the energy saved by decreasing the supply voltage is wasted by the **DC-DC Converter** .

In particular it is important to take into account the micro-controllers that in this type of devices have a repetitive behavior. They work staying long times in sleep mode

[1] In this equation f is the switching frequency, C_L is an equivalent capacitor, and V_{DD} is the supply voltage.

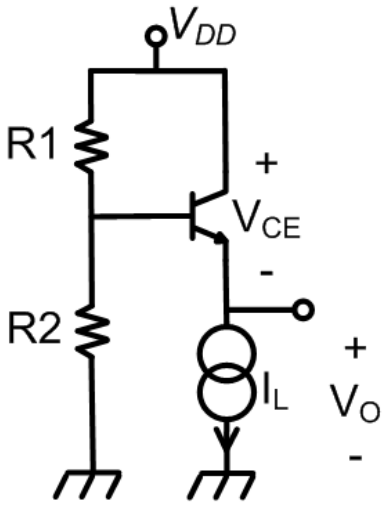


Figure 1.1: DC/DC converter implemented with an emitter follower.

with a consumption of some μA and then they wake up to make some calculations and transmit information, with a typical consumption of some hundred of μA. For example the $PIC16(L)F1826/27$ is a **Ultra Low Power** Micro-controller from Microchip that has a consumption of $75\mu A/MHz_{@V_{DD}=1,8V}$ in active mode. In the sleep mode it has a consumption of $30nA$ but in most cases a time reference is needed so a timer is kept on all the time. The timer consumes $0{,}6\mu A_{@32kHz}$ so this is a more real sleep mode consumption. The $MSP430$ is a family of Micro-controllers from Texas Instruments that has a consumption of $220\mu A/MHz_{@V_{DD}=2,2V}$ and $0{,}5\mu A$ in stand-by mode. So it is very important to have converters with good efficiency at these orders of currents.

A basic DC/DC converter can be an emitter follower as the one shown in Figure 1.1. The problem with this type of converter is that if we need to decrease the voltage to supply a digital circuit to improve the consumption, all the energy saved at the load is dissipated by the transistor, so there is no energy saved after all. Therefore for greater efficiency components capable of storing energy and then delivering it are used.

A very important family of such converters is the inductor-based converters such as buck and boost. The problem with them is that inductors are not suitable for integration mainly because they have a poor quality factor (Q), so they are not a good option for fully integrated DC/DC converters. In [3] a buck converter was presented with a poor achieved efficiency and a special technology was used in the capacitor fabrication and the inductor isolation. Also the design was made for much higher currents (in the order of mA). [4] presents a buck converter and said that the most complicated design issue is the inductor and uses a special technology that builds the inductor out of the chip but places it into the package. The power delivered by the converter is up to $0{,}5W$ so it is much higher than the previously mentioned. Then in [5] two techniques where used to avoid the low Q of the inductors and a good efficiency was achieved, but for much higher power too. In [6] a good efficiency was achieved but again for much higher power. As a conclusion, in the literature there are some works but most of them men-

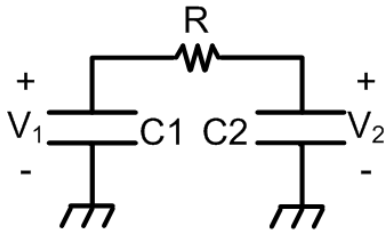


Figure 1.2: Capacitor to capacitor charge transfer.

tion difficulties or the need to use special technologies to build this type of converters on chip. On the other hand, the converters that achieve a good efficiency are designed for much higher power than the needed in **Ultra Low Power** applications. So this type of converters is not suitable for our aim.

To avoid both problems (low efficiency for low currents and lack of easy integration capability), switched capacitor converters are used. This type of converters are based in the fact that energy transfer between capacitors can be made with an efficiency as close to $100\,\%$ as needed [2]. If we consider the capacitors shown in Figure 1.2 where the objective is to transfer energy from $C1$ to $C2$ through the resistance R, and we have the initial conditions: $V1_i = V_i$ and $V2_i = V_i - \Delta V$, it is possible to demonstrate that the energy delivered to C2 is given by equation 1.2. It is also posible to demonstrate that the dissipated energy in the resistor is given by equation 1.3. The efficiency is the energy delivered to $C2$ over the energy consumed from the source ($C1$ in our case). So efficiency is given by equation 1.4[3]. As E_{Lost} decreases faster than $\Delta E2$ when $\Delta V \to 0$, the asymptotic efficiency is $100\,\%$ ($\eta \to 1$) if $\Delta V \approx 0$.

$$\Delta E2 = \frac{C1.C2}{C1+C2}.\left(V_i.\Delta V - \frac{\Delta V^2}{2}.\left(\frac{C1+2.C2}{C1+C2}\right)\right) \tag{1.2}$$

$$E_{Lost} = \frac{C1.C2.\Delta V^2}{2.(C1+C2)} \tag{1.3}$$

$$\eta = \frac{\Delta E2}{\Delta E2 + E_{Lost}} \tag{1.4}$$

For the reason mentioned above we can conclude that **Switched Capacitor Converters** are the best option for our aim. So these are the converters studied in this thesis.

For low-level currents (below 1mA), comercial converter's efficiency is in general poor because they are designed for higher currents. So it is difficult to get a comercial **DC-DC Converter** to decrease the supply voltage efficiently for **Ultra Low Power** circuits (in the order of μA as mentioned above).

[2] In this analysis we are just considering conduction losses. As will be see in the next section there are more losses that put a lower asymptotic limit in the efficiency.

[3] Equations 1.2, 1.3 and 1.4 are derived in the appendix B.

However, academic research has been developing the area for some years. [7] is a very important work that achieves very good efficiency levels for **Ultra Low Power** applications. [8] is the most recent work that achieves similar results in terms of efficiency using different architecture and control logic. [9] has a good efficiency in relation with the conversion ratio (62 % of efficiency with a 1/5 conversion ratio) but has just one conversion ratio. [10] has the peak of efficiency of $66{,}7\,\%$ when the conversion ratio is approximately $0{,}6$, but the controller consumes $147{,}5\mu W$[4] despite using subthreshold logic. The specifications said that the minimum power to the load is $400\mu W$ that is two or three orders higher than the consumption of a micro-controller in sleep mode. Then, [11] has an single output voltage ($444mV$) and a peak efficiency of $56\,\%$ with a load current of $285nA$. Furthermore, if we supply a digital circuit with $444mV$ we are working in the subthreshold region for the technology used. [12] achieves an efficiency from $37\,\%$ to $56\,\%$ but for currents from $1\mu A$ to $4\mu A$ and has just one output voltage level.

All these works use particular architectures that are hardly able to include another conversion ratio. This work presents a novel architecture for **Switched Capacitor Converters** that has the advantage of being modular and able to include more conversion ratios if necessary. This feature makes the architecture very appropriate for **Dynamic Voltage Scaling** . This is achieved presenting similar features in terms of efficiency in comparison with previous works. A novel technique to reduce dominant losses (parasitic capacitances losses) is presented, that has the particularity of reducing such losses as the number of conversion ratios is increased.

Summarizing the target application characteristics, the list of requirements for this work is:

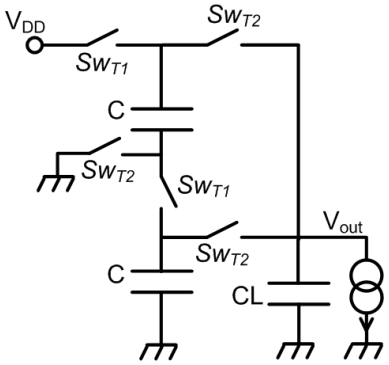
- Input voltage $2{,}8V$
- Current load $1\mu A$ - $100\mu A$
- Multiple conversion ratios with the same architecture
- High efficiency ($> 60\,\%$)

1.2. General Considerations for Switched Capacitor Converters

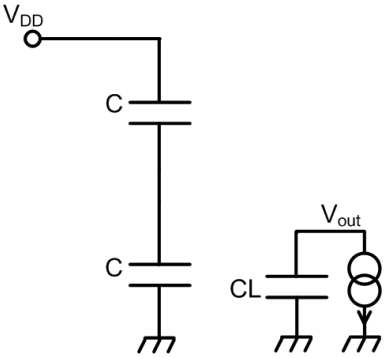
In a **Switched Capacitor Converter** there are several capacitor configurations and the times of duration of each configuration are called phases. An example of a basic **Switched Capacitor Converter** is shown in Figure 1.3. In Sub-Figure 1.3(a) the converter is shown with all the switches opened, then in Sub-Figure 1.3(b) the converter is shown in the configuration of phase one, and last in Sub-Figure 1.3(c) in the phase two.

During phase one the two capacitors of the converter are connected in series to the voltage source and each one is charged at $\frac{V_{DD}}{2}$. The output voltage is kept by the capacitor C_L. Then in the second phase the two capacitors are connected in parallel to

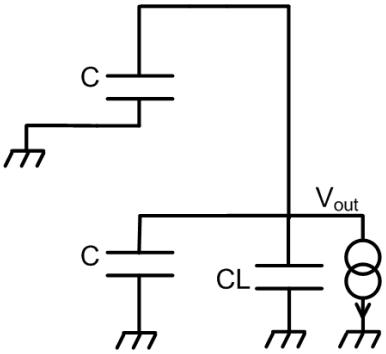
[4] Remember that the power consumption of the micro-controllers previously mentioned is approximately this value.



(a) Divider-by-two converter



(b) Divider-by-two converter during the first phase configuration



(c) Divider-by-two converter during the second phase configuration

Figure 1.3: Two phases divider-by-two **Switched Capacitor Converter** basic example

capacitor C_L and deliver to it the energy lost in the first phase and the needed by the load.

This cycle is repeated at a frequency f_{sw}. If the frequency and capacitors are such that the voltage in capacitors are essentially constant, the lost energy is negligible and the efficiency of the converter is close to $100\,\%$.

This and other configurations can be seen in [7].

1.2.1. Losses In Switched Capacitor Converters

In the previous analysis a $100\,\%$ asymptotic efficiency was mentioned. This was without considering some effects that cause an energy loss and a lower limit in the efficiency. This section analyzes the main types of losses.

Conduction Losses

As stated above, transfering charge from one capacitor to another (or from the supply voltage to a capacitor) with a lower voltage has a loss in the resistance of the switch involved in the process. As can be seen in equations (1.2), (1.3) and (1.4) the smaller is the voltage difference (ΔV) the more negligible are these losses. This type of energy loss is named E_{cond}.

Gate-drive Losses

To drive the gate of the switches that implement the different phases of the converter there is a cost of energy. So to minimize this losses it is necessary to implement the switches as small as possible. This type of energy loss is named E_{gates}.

Parasitic Capacitance Losses

When a floating capacitor is implemented in an **Integrated Circuit** some parasitic capacitances between the plates of the capacitor and the substrate appear. When the capacitor changes the voltage of the plates with respect to the substrate, energy is wasted to charge and discharge these parasitic capacitances, because this energy is not delivered to the load.

An example of floating capacitor implementation is with a poly1-poly2 capacitor. Figure 1.4 shows the capacitor and the parasitic capacitances involved.

Another way to implement a floating capacitor is using a PMOS capacitor (in a N-Well technology)[5]. This implementation has the advantage that the capacity per unit area is higher than the first option (POLY1-POLY2), but has the disadvantage that it has a non-linear behavior. The implementation is shown in Figure 1.5 where it can be seen that Drain, Source, and Bulk are one plate of the capacitor and the Gate is the other. The NWell-Substrate diode parasitic capacitance appears in this case.

[5] If we are using a N-Well technology it is necessary to use a PMOS transistor because the capacitor must be floating. As the NWell can float with respect to ground we must use a PMOS capacitor.

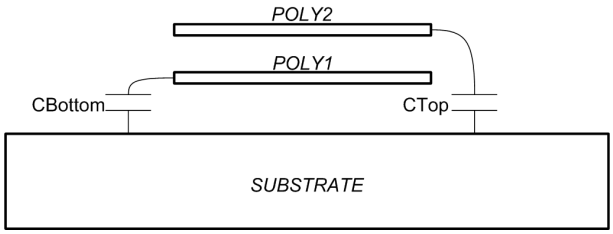


Figure 1.4: Bottom and top parasitic capacitances in a poly-poly capacitor.

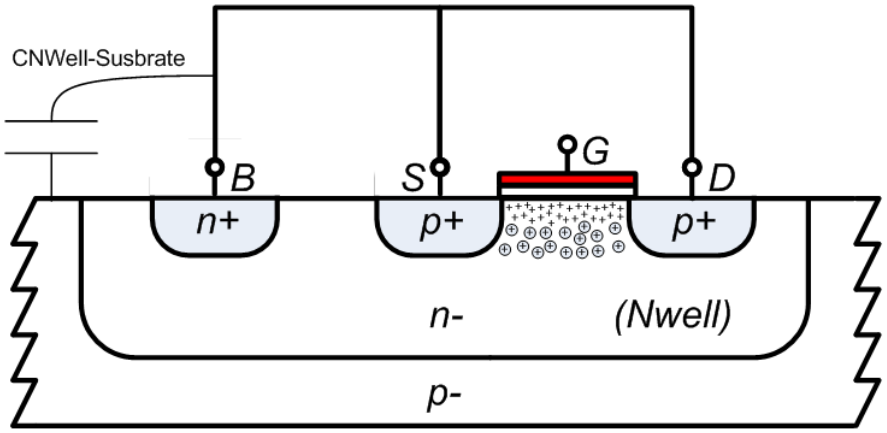


Figure 1.5: PMOS capacitor implementation and parasitic capacitances.

The energy lost due to the charging and discharging of these parasitic capacitances is named E_{par}.

Logic Losses

To manage the switches of the converter a sequential logic is needed. The energy supplied to the logic circuits is not delivered to the load so it is important to minimize these losses to have a good efficiency mainly when the power delivered to the load is low. This type of energy lost is named E_{logic}. We will include in this term also the energy consumed by the analog circuits of the control block.

1.2.2. Efficiency

As the objective of a **Switched Capacitor Converter** is to deliver energy to a device using a different voltage than the input one, the efficiency is defined in terms of energy. So the efficiency is the ratio between energy delivered by the converter to the load and the energy taken by the converter from the supply voltage:

$$\eta = \frac{E_{out}}{E_{in}} = \frac{E_{load}}{E_{load} + E_{loss}} \tag{1.5}$$

where

$$E_{loss} = E_{cond} + E_{gates} + E_{par} + E_{logic} \tag{1.6}$$

and E_{load} is the energy delivered to the load.

1.2.3. Output Resistance

Figure 1.6 shows an equivalent circuit for a general **Switched Capacitor Converter** . It is not possible to have a general theory to derive the output resistance R_{OUT}. However it is posible to develop a general theory to calculate this resistance in the two limit modes that a **Switched Capacitor Converter** can work. These modes are the Slow Switching Limit (SSL from now on) and Fast Switching Limit (FSL from now on) that are discussed in the Chapter 2 of [13].

It is considered that a given **Switched Capacitor Converter** is working in SSL when the switching frequency is slow enough to consider that currents are impulsive, or equivalently each phase of the converter has a time duration much bigger than the time constants (τ) of the different topologies of the circuits. In this limit an equivalent output resistance (R_{SSL}) can be calculated, this calculation can be made with a general theory that can be applied in all **Switched Capacitor Converters** . This equivalent resistance has the particularity of being inversely proportional to the switching frequency as can be seen in equation (1.7). The constant K_{SSL} is a function of the capacitor values, number of phases of the converter and the topology. In particular it is important to highlight that K_{SSL} is a sum where each term is inversely proportional to a capacitor of the converter.

$$R_{SSL} = \frac{K_{SSL}}{f_{Sw}} \tag{1.7}$$

On the other hand, it is considered that a given **Switched Capacitor Converter** is working in FSL when the switching frequency is fast enough to consider that currents are constant, or equivalently each phase of the converter has a time duration much lower than the time constants (τ) of the different topologies of the circuits. Again in this limit an equivalent output resistance (R_{FSL}) can be calculated with a general theory that can be applied in all **Switched Capacitor Converters** . This equivalent resistance has the particularity of being independent of the switching frequency. The value of this resistance depends of the switches resistance, the number of phases of the converter and the topology.

As mentioned above it is not possible to develop a general theory to calculate the output resistance in the range of frequencies where none of the two modes are valid. However an accepted approximation can be used as shows the equation (1.8).

$$R_{OUT} \simeq \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{1.8}$$

A deeper analysis of the output resistance calculations can be seen in the chapter two of [13].

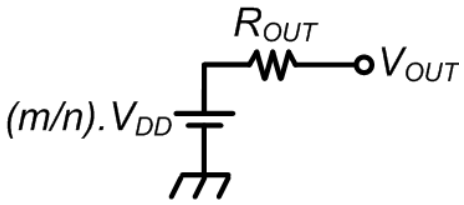


Figure 1.6: **Switched Capacitor Converter** equivalent circuit.

CHAPTER 2

Proposed Architecture

The general idea of the architecture proposed in this thesis is to have n equal capacitors connected in series and another capacitor connected in parallel with the load (C_L from now on). One end of the series is always connected to ground. The other end is connected to the source during one phase. The load and C_L are connected to an alternative node during the other phase. Therefore, the converter has two phases and $n-1$ conversion ratios (as many as intermediate nodes in the series). Figure 2.1 shows a particular case with $n = 5$ and a conversion ratio of $\frac{3}{5}$.

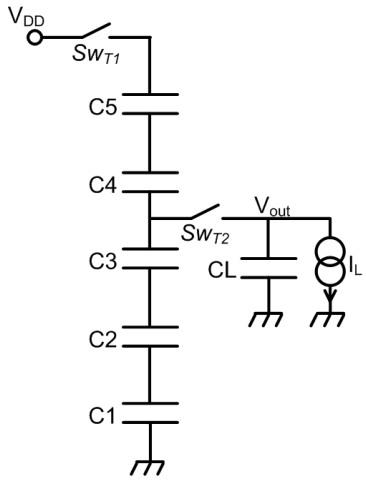
In the first phase ($T1$ from now on) shown in the Sub-Figure 2.1(b) the source (V_{DD}) is connected to the capacitor series, so the converter takes energy from the source and all the capacitors in the series have a voltage $\frac{V_{DD}}{n}$. In this phase C_L gives charge to the load and keeps the output voltage V_{OUT}.

In the second phase ($T2$ from now on) shown in Sub-Figure 2.1(c) one of the intermediate nodes of the series is connected to the load and the source is disconnected. So the converter gives charge to the load and returns to C_L the charge taken by the load during $T1$ [1]. The conversion ratio is defined by the node where the load is connected during this phase.

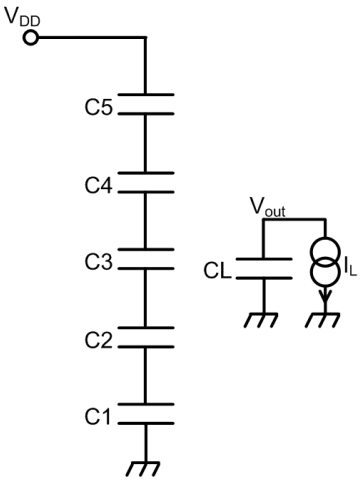
Sub-Figure 2.1(a) shows the series of capacitors $C1..C5$, the capacitor connected to the load C_L, the load represented by a current source, and the switches $SwT1$ and $SwT2$ used in phases $T1$ and $T2$ respectively. Then in Sub-Figures 2.1(b) and 2.1(c) are shown respectively the configuration in the two phases. If for example we want to have a conversion ratio of $\frac{4}{5}$ we must connect the output to the node between $C4$ and $C5$.

The problem here is that during $T2$ the capacitor composed by the series $C1..C3$ is discharged (gives charge to the load and C_L) while the capacitor composed by the series of $C4$ and $C5$ keeps the same charge. This difference of charge remains unchan-

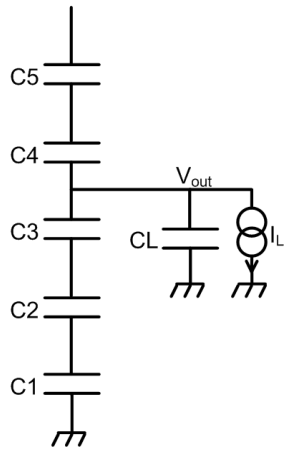
[1] Expressions $T1$ and $T2$ are used to represent both the phase and the duration of each.



(a) Basic Converter



(b) Configuration during T1



(c) Configuration during T2

Figure 2.1: Example of converter with n = 5 and conversion ratio of 3/5

ged when in the next phase $T1$, the total series is connected to the supply voltage and the sum of voltages in the five capacitor is V_{DD}. Therefore the voltage in the series $C1..C3$ will decrease every cycle and the output voltage too. The voltage in the series of capacitors $C4$ and $C5$ has the opposite effect and will increase every cycle . So it is necessary a way to replace this charge in the node where the load is connected.

To solve this problem, capacitors are rotated of position in the ring. So instead of thinking about a series of capacitors it is better to imagine a ring which can be opened in every node. All the capacitors of the ring are associated to a switches configuration that implement a **Basic Capacitor Cell** . Figure 2.2 shows that cell.

It can be seen that the top plate of the capacitor can be connected to the input and to the output through the switches $SwT1$ and $SwT2$. It also shows that the ring can be opened with the switch $SwInter$ and can be connected to ground through the switch $SwGnd$.

Figure 2.3 shows an example with $n = 5$ where the ring is composed by five **Basic Capacitor Cells** , Figure 2.3(a) shows the ring with all the switches opened. Then in 2.3(b) and 2.3(c) the configuration of the ring before and after a rotation are shown. In the first one the ring is opened in the **Basic Capacitor Cell** of capacitor $C5$ and the output is connected through the **Basic Capacitor Cell** of capacitor $C3$. After the rotation the ring is opened in the **Basic Capacitor Cell** of capacitor $C4$ and the output is connected through the **Basic Capacitor Cell** of capacitor $C2$. In this way all capacitors will be connected to the supply voltage in a moment and will recover the charge.

The rotation of the ring causes a significant loss in parasitic capacitances, so there is a trade-off between avoiding the rotation of the ring to minimize the mentioned losses, and the need to rotate the ring to replace the charge to the nodes where the load is connected. This effect is illustrated in Sub-Figure 2.11(a) showing the output voltage (V_{OUT}). In the first phase $T1$ (bounded with two dotted lines) the ring is being rotated and the load is taking charge from C_L, so the output voltage is decreasing. In the next phase $T2$ (bounded with two dotted lines too) the output voltage is increased by the charge given by converter to C_L and the load. This process is repeated eight times before the next rotation. As can be seen in the first three periods $T1 + T2$ the output voltage is increased, but because the discharging process above mentioned in the next five periods the same will decrease. In this example the conversión ratio is $\frac{4}{5}$ and the supply voltage (V_{DD}) is 2.8V. The rest of the waveforms will be explained next.

A discussion on which is the best way to implement the rotation will be introduced in Section 2.3 after the parasitic capacitances losses are analyzed.

2.1. Capacitors Implementation

Since the capacitors of the ring have essentially the same bias voltage it is posible to use non-linear capacitors and keep the ratio between them (all equal in our case). So it is possible to use in parallel with the POLY1-POLY2 capacitors a PMOS capacitor. This increases the capacitance per unit area because it is posible to build a POLY1-POLY2 capacitor above a PMOS capacitor. The load capacitor (C_L) needs no matching so it is possible to use a combined device too.

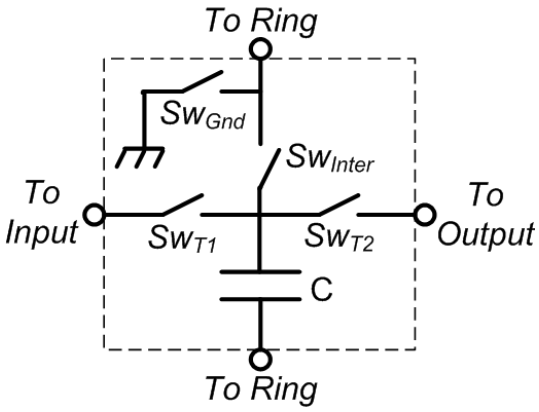


Figure 2.2: **Basic Capacitor Cell**

This has an advantage because the bottom parasitic capacitance (POLY1-NWell) can be connected in parallel with the main capacitor and the top parasitic capacitance (POLY2-NWell) is short-circuited (see Figure 1.4). As a disadvantage the NWell-Substrate parasitic capacitance appears. Figure 2.4 shows the composed capacitor and the parasitic capacitance.

2.2. Charge Transfer Analysis

Figure 2.5 shows a general series of n equal capacitors of value C and the load capacitor C_L. If we have a conversion ratio of $\frac{m}{n}$ the equivalent circuit is a series of two capacitors: $C1_{eq} = \frac{C}{m}$ and $C2_{eq} = \frac{C}{n-m}$. They can be seen in Figure 2.5(b).

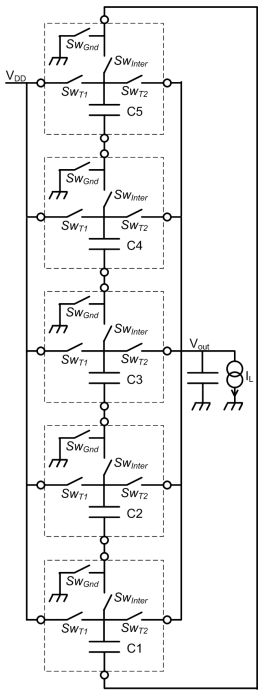
To understand the energy transmission in a cycle we will consider three phases: $T1$ that gives us the initial conditions, $T2$ that transfers charge to the load and C_L, and $T1$ again because it is the phase when the supply voltage replaces the energy delivered by the converter to the load.

After the first phase $T1$, when the source V_{DD} is connected, $C1_{eq}$ and $C2_{eq}$ have a charge $Q1_i$ and $Q2_i$ respectively. To make a general analysis $Q1_i$ and $Q2_i$ are not necessarily equal. So we have the equation:

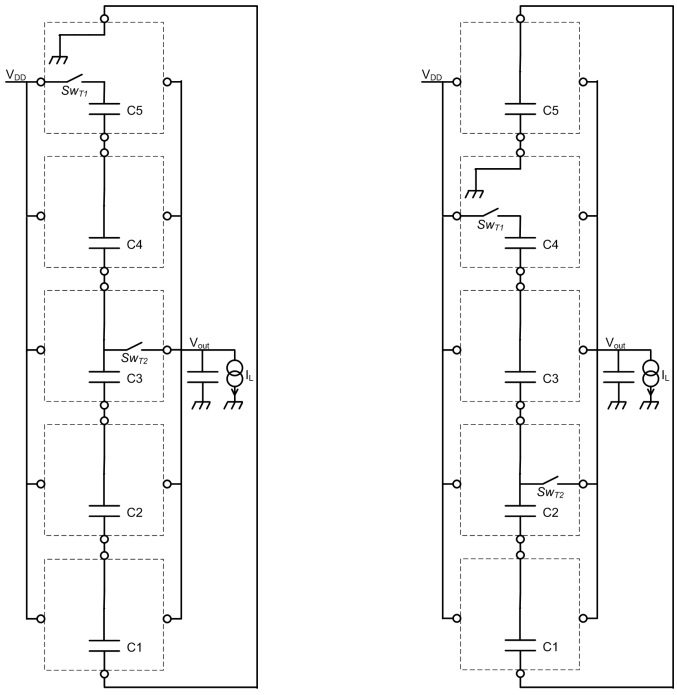
$$V_{DD} = \frac{Q1_i}{C1_{eq}} + \frac{Q2_i}{C2_{eq}} \tag{2.1}$$

During the phase $T2$ the load and C_L take a charge ΔQ from $C1_{eq}$. [2]. Thus, the difference between the charge of $C2_{eq}$ and $C1_{eq}$ is ΔQ more than at the beginning. So we have the equation:

[2]The charge ΔQ is the demanded by the load during $T2$ and the necessary to replace the charge taken by the load from C_L during one $T1$. So it is the total charge taken by the load in a cycle $T1 + T2$.



(a) Ring with five **Basic Capacitor Cells**



(b) Before rotation

(c) After rotation

Figure 2.3: Example of rotation in a five **Basic Capacitor Cells** ring

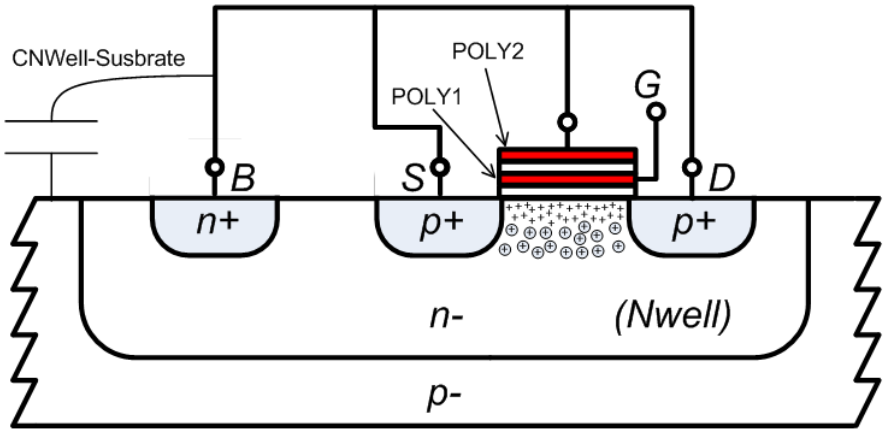
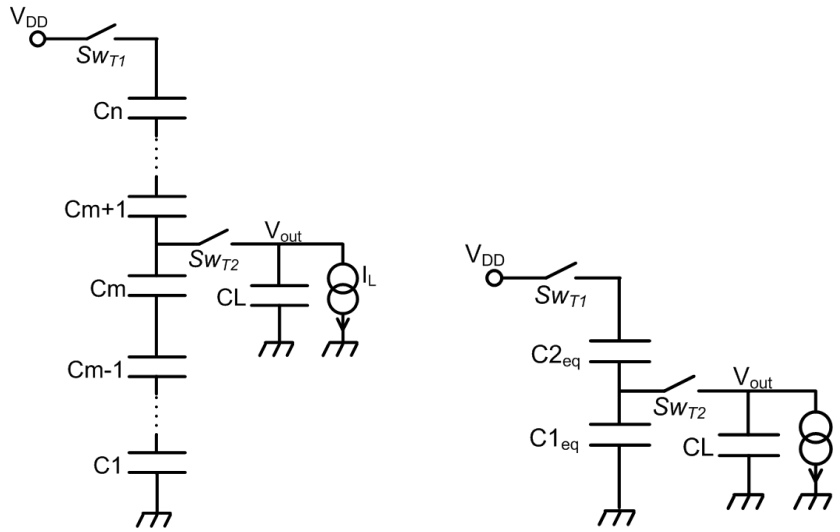


Figure 2.4: POLY1-POLY2 - PMOS composed capacitor.



(a) General converter (b) General converter equivalent

Figure 2.5: Power Transmission

$$Q2_f - Q1_f = Q2_i - Q1_i + \Delta Q \tag{2.2}$$

As $Q1_f$ and $Q2_f$ are the charge in $C1_{eq}$ and $C2_{eq}$ respectively in the second considered phase $T1$ they meet the following equation:

$$V_{DD} = \frac{Q1_f}{C1_{eq}} + \frac{Q2_f}{C2_{eq}} \tag{2.3}$$

Now from (2.2) and (2.3)

$$V_{DD} = \frac{Q2_f - Q2_i + Q1_i - \Delta Q}{C1_{eq}} + \frac{Q2_f}{C2_{eq}} \tag{2.4}$$

Thus

$$V_{DD} - \frac{Q1_i}{C1_{eq}} = Q2_f.\left(\frac{1}{C1_{eq}} + \frac{1}{C2_{eq}}\right) - \frac{Q2_i}{C1_{eq}} - \frac{\Delta Q}{C1_{eq}} \tag{2.5}$$

And from (2.1) we have that

$$\frac{Q2_i}{C2_{eq}} = Q2_f.\left(\frac{1}{C1_{eq}} + \frac{1}{C2_{eq}}\right) - \frac{Q2_i}{C1_{eq}} - \frac{\Delta Q}{C1_{eq}} \tag{2.6}$$

Then

$$Q2_i.\left(\frac{1}{C1_{eq}} + \frac{1}{C2_{eq}}\right) = Q2_f.\left(\frac{1}{C1_{eq}} + \frac{1}{C2_{eq}}\right) - \frac{\Delta Q}{C1_{eq}} \tag{2.7}$$

Or

$$Q2_f = Q2_i + \Delta Q.\left(\frac{C2_{eq}}{C1_{eq} + C2_{eq}}\right) \tag{2.8}$$

Since the variation in the charge of $C2_{eq}$ is given by the source, the charge taken from the source during the second considered phase $T1$ to replace the charge taken by the load and C_L during phase $T2$ is:

$$\Delta Q_{V_{DD}} = \Delta Q.\left(\frac{C2_{eq}}{C1_{eq} + C2_{eq}}\right) \tag{2.9}$$

For all devices we have that:

$$\Delta E = \int V.I.dt \tag{2.10}$$

In the case of the source the voltage is constant so the delivered energy is:

$$\Delta E_{V_{DD}} = \int V_{DD}.I.dt = V_{DD}.\int I.dt = V_{DD}.\Delta Q_{V_{DD}} \tag{2.11}$$

From (2.9) and (2.11)

$$\Delta E_{V_{DD}} = V_{DD}.\Delta Q.\left(\frac{C2_{eq}}{C1_{eq} + C2_{eq}}\right) \tag{2.12}$$

To calculate the energy taken by the load in the cycle we do not have a constant voltage, but if we think in capacitors as big as necessary to have essentially a constant voltage in all of them we can say that the equation (2.10) in the case of the load is

$$\Delta E_{Load} = V_{OUT}.\Delta Q \tag{2.13}$$

As can be seen from figure 2.5 the no load output voltage is $V_{OUT}^{NL} = V_{DD}.\left(\frac{C2_{eq}}{C1_{eq}+C2_{eq}}\right)$. As capacitors are considerer as big as necessary we have that $V_{OUT} = V_{OUT}^{NL}$. So using equation 2.13:

$$\Delta E_{Load} = V_{DD}.\left(\frac{C2_{eq}}{C1_{eq}+C2_{eq}}\right).\Delta Q \tag{2.14}$$

And the efficiency is:

$$\eta = \frac{\Delta E_{Load}}{\Delta E_{V_{DD}}} = 1 \tag{2.15}$$

As we have considered a general case it is possible to conclude that the architecture proposed has an asymptotic ideal efficiency of $100\,\%$ for all the conversion ratios.

2.3. Parasitic Capacitances Losses

As will be seen next these losses are the main source of loss so it is very important to have a good understanding of the subject. Parasitic capacitances losses happen when the ring is rotated. So to understand which is the best way to rotate the ring it is very important to know the dependence of these losses with the rotation process.

Figure 2.6 shows the **Basic Capacitor Cell** with and without the parasitic capacitances which appear in 2.6(b) as C_{Par1} and C_{Par2}[3].

C_{Par1} is composed of the parasitic capacitances of the switches $SwT1$, $SwT2$, $SwInter$, and the parasitic capacitance of the NWell-Substrate diode of the PMOS capacitor[4]. C_{Par2} is composed of the parasitic capacitances of the switches $SwGnd$ and $SwInter$. So C_{Par1} and C_{Par2} are described by equations (2.16) and (2.17) respectively.

$$C_{Par1} = C_{ParSwT1} + C_{ParSwT2} + C_{ParSwInter} + C_{NWell-Sust} \tag{2.16}$$

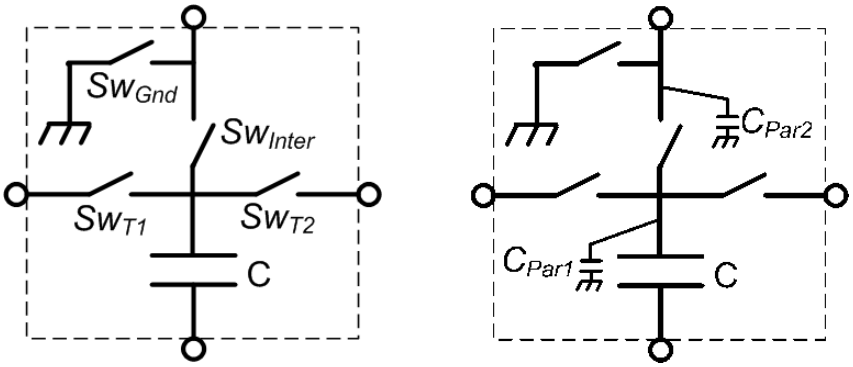
and

$$C_{Par2} = C_{ParSwGnd} + C_{ParSwInter} \tag{2.17}$$

As variation of energy in a capacitor is given by equation (2.18), to calculate the energy consumed in a rotation we need to know the voltage in every node of the ring before and after the rotation. To see this we must look at Figure 2.7. In 2.7(a) and

[3]Note that there are more parasitic capacitances but the ones shown in the figure 2.6(b) are the only ones that consume energy in the rotation. The other parasitic capacitances of the switches are connected to fix voltage nodes.

[4]Remember that capacitor C is composed by a poly-poly capacitor in parallel with a PMOS capacitor (See Figure 2.4).



(a) Basic capacitor cell without parasitic capacitances

(b) Basic capacitor cell with parasitic capacitances

Figure 2.6: Parasitic capacitance of a **Basic Capacitor Cell**

2.7(b) we can see the ring configuration before and after a rotation respectively. We will analyze the general case when the ring is open in the **Basic Capacitor Cell** of the capacitor Cn and after the rotation we open the ring in the **Basic Capacitor Cell** of a generic Cp capacitor of the ring.

$$\Delta E_C = \frac{C}{2}.\left(V_f^2 - V_i^2\right) \tag{2.18}$$

In Figure 2.7(a) we can see that the bottom plate of capacitor C_1 is connected to ground through the switch $SwGnd$ of the capacitor C_n. The input (V_{DD}) is connected during $T1$ through the switch $SwT1$ of the capacitor C_n. So it is simple to see that the voltage in the top plate of the capacitor C_1 is $V_{DD}.\frac{1}{n}$, in C_2 is $V_{DD}.\frac{2}{n}$, etc. So for C_{Par1} we have that:

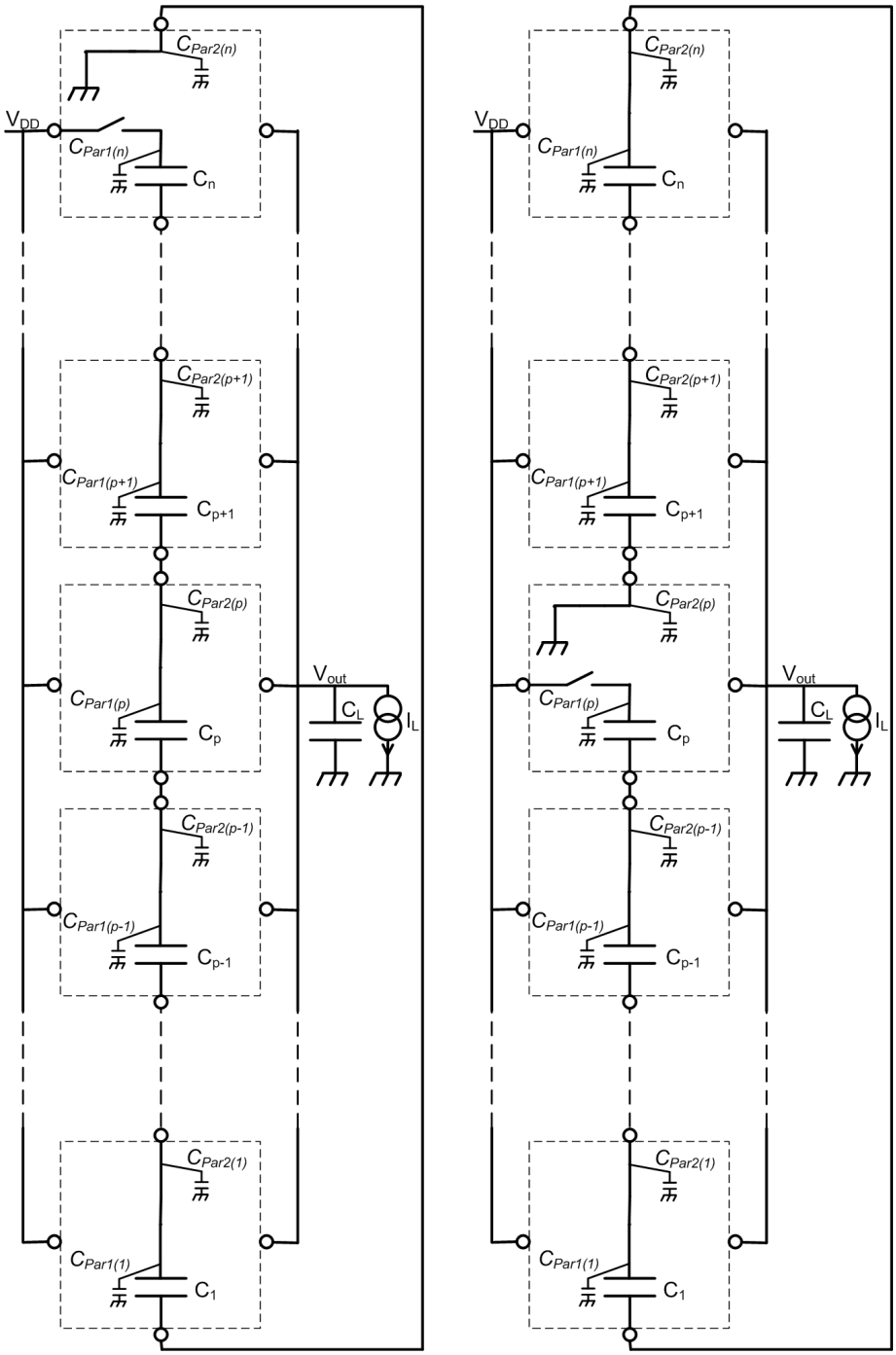
$$V_{C_{Par1}i}(k) = V_{DD}.\left(\frac{k}{n}\right); \quad \forall k = 1:n \tag{2.19}$$

In the case of C_{Par2} it is the same with the exception of C_n because this node is connected to ground. So for C_{Par2} we have that:

$$V_{C_{Par2}i}(k) = \begin{cases} V_{DD}.\left(\frac{k}{n}\right) & \forall k = 1:n-1 \\ 0 & k = n \end{cases} \tag{2.20}$$

In Sub-Figure 2.7(b) we can see that the bottom plate of C_{p+1} is connected to ground through the switch $SwGnd$ of the capacitor C_p. The input (V_{DD}) is connected during $T1$ through the switch $SwT1$ of the capacitor C_p. We can see that the voltage in the top plate of C_{p+1} is $V_{DD}.\frac{1}{n}$ and so on to C_n that has a voltage in the top plate of $V_{DD}.\frac{n-p}{n}$. Equally we can see that top plate of C_p is V_{DD} and so on to C_1 who has a voltage in the top plate of $V_{DD}.\frac{n-p+1}{n}$. Summarizing the final voltage of every parasitic capacitor C_{Par1} is:

$$V_{C_{Par1}f}(k) = \left\{ \begin{matrix} V_{DD}.\left(\frac{k+n-p}{n}\right) & \forall k = 1:p \\ V_{DD}.\left(\frac{k-p}{n}\right) & \forall k = p+1:n \end{matrix} \right\} 0 < p < n \tag{2.21}$$



(a) Ring before rotation (b) Ring after rotation

Figure 2.7: Ring configuration changes in a rotation

In the case of C_{Par2} it is the same with the exception of C_p because this node is connected to ground. So for C_{Par2} we have that:

$$V_{C_{Par2}f}(k) = \left\{ \begin{matrix} V_{DD}.\left(\frac{k+n-p}{n}\right) & \forall k = 1:p-1 \\ V_{DD}.\left(\frac{k-p}{n}\right) & \forall k = p:n \end{matrix} \right\} 0 < p < n \tag{2.22}$$

Thus from equations (2.18), (2.19) and (2.21) we have that:

$$\Delta E_{C_{Par1}}(k) = \frac{C_{Par1}}{2}.V_{DD}^2.\left\{ \begin{matrix} \left[\left(\frac{k+n-p}{n}\right)^2 - \left(\frac{k}{n}\right)^2\right] & \forall k = 1:p \\ \left[\left(\frac{k-p}{n}\right)^2 - \left(\frac{k}{n}\right)^2\right] & \forall k = p+1:n \end{matrix} \right\} 0 < p < n \tag{2.23}$$

From equation (2.23) we can see that the energy variation in parasitic capacitors from C_1 to C_p is positive and negative in the rest. This is because in the first case parasitic capacitors are receiving energy form the source and in the second one they are throwing the energy to ground. So to calculate the energy consumed from the source we have:

$$\Delta E_{C_{Par1}Total} = \sum_{k=1}^{p} \Delta E_{C_{Par1}}(k) = \frac{C_{Par1}}{2}.V_{DD}^2.\sum_{k=1}^{p}\left[\left(\frac{k+n-p}{n}\right)^2 - \left(\frac{k}{n}\right)^2\right] \tag{2.24}$$

And from equations (2.18), (2.20) and (2.22) we have that:

$$\Delta E_{C_{Par2}}(k) = \frac{C_{Par2}}{2}.V_{DD}^2.\left\{ \begin{matrix} \left[\left(\frac{k+n-p}{n}\right)^2 - \left(\frac{k}{n}\right)^2\right] & \forall k = 1:p-1 \\ \left[\left(\frac{k-p}{n}\right)^2 - \left(\frac{k}{n}\right)^2\right] & \forall k = p:n-1 \\ \left[\left(\frac{k-p}{n}\right)^2 - 0\right] & k = n \end{matrix} \right\} 0 < m < n \tag{2.25}$$

From equation (2.25) we can see that the energy variation in parasitic capacitors from C_p to C_{n-1} is negative and positive in the rest. This is because in the first case parasitic capacitors are throwing to ground the energy and in the second one they are receiving energy form the source. In steady-state the energy received form the source is equal to the one thrown to ground. So to calculate the energy consumed from the source we can do it using the negative terms of equation (2.25) and multiplying them by -1. So we have that:

$$\Delta E_{C_{Par2}Total} = \sum_{k=p}^{n-1} \Delta E_{C_{Par2}}(k) = \frac{C_{Par2}}{2}.V_{DD}^2.\sum_{k=p}^{n-1}\left[\left(\frac{k}{n}\right)^2 - \left(\frac{k-p}{n}\right)^2\right] \tag{2.26}$$

From equations (2.24) and (2.26) we can see that the consumption of a rotation of the ring has a dependency with p. This is equivalent to say that it has a dependency with the number of places that the capacitors are shifted in each rotation. To know which is

the best way to rotate the ring it is enough to know the dependence with p of the sums that appear in both equations. These sums will be called $sumCPar1$ and $sumCPar2$ respectively. Figure 2.8 shows the value of the sums as function of p for converters of five, six, and seven **Basic Capacitor Cells** , where is clear that the best choice is to shift one place each capacitor in each rotation so the election is $p = n - 1$[5].
So for the choice taken equations (2.24) and (2.26) become:

$$\Delta E_{C_{Par1}Total} = \frac{C_{Par1}}{2}.V_{DD}^2.\sum_{k=1}^{n-1}\left[\left(\frac{k+1}{n}\right)^2 - \left(\frac{k}{n}\right)^2\right]$$

or

$$\boxed{\Delta E_{C_{Par1}Total} = \frac{C_{Par1}}{2}.V_{DD}^2.\left(1 - \frac{1}{n^2}\right)} \tag{2.27}$$

and

$$\Delta E_{C_{Par2}Total} = \frac{C_{Par2}}{2}.V_{DD}^2.\sum_{k=n-1}^{n-1}\left[\left(\frac{k}{n}\right)^2 - \left(\frac{k-(n-1)}{n}\right)^2\right]$$

or

$$\boxed{\Delta E_{C_{Par2}Total} = \frac{C_{Par2}}{2}.V_{DD}^2.\left(\frac{n-1}{n}\right)^2} \tag{2.28}$$

Thus

$$\boxed{\Delta E_{C_{Par}Total} = \frac{C_{Par1}}{2}.V_{DD}^2.\left(1 - \frac{1}{n^2}\right) + \frac{C_{Par2}}{2}.V_{DD}^2.\left(\frac{n-1}{n}\right)^2} \tag{2.29}$$

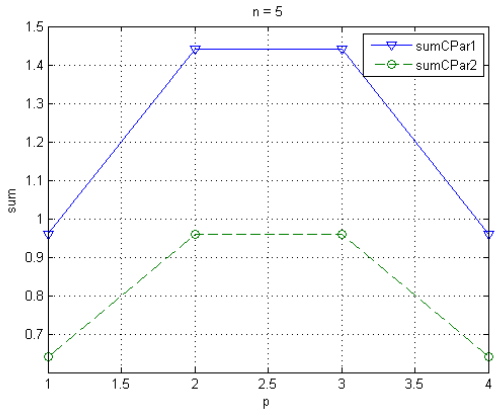
2.4. Rotation Technique to Reduce Parasitic Capacitances Losses

Since parasitic capacitances losses are the main reason for losses in the converter and therefore the fall in efficiency, a detailed analysis of this issue for the chosen case of rotation ($p = n - 1$) is made in this section. Then the implemented technique to decrease these losses is presented.

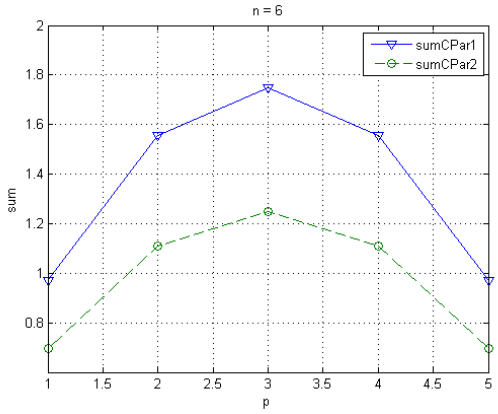
Figure 2.9 shows the state of the parasitic capacitances before and after the rotation. In Sub-Figure 2.9(a) the state of all the parasitic capacitances before the rotation is shown. C_{Par1_n} voltage is V_{DD} and C_{Par2_n} voltage is zero[6]. Parasitic capacitances

[5] From Figure 2.8 it is clear that it is exactly the same to choose $p = 1$ or $p = n - 1$ so the election $p = n - 1$ is arbitrary. Furthermore this choice has no impact on other aspects as logic or switching consumption, etc.

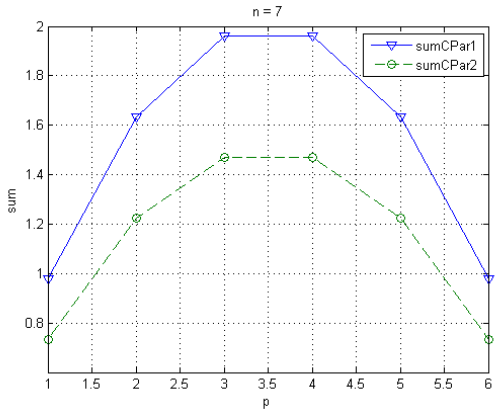
[6] Remember that parasitic capacitances C_{Par1} and C_{Par2} of a **Basic Capacitor Cell** are short-circuited if the interconnection switch is closed. See Figure 2.6.



(a) SumCPar1 and SumCPar2 for a five **Basic Capacitor Cells** converter as function of p.



(b) SumCPar1 and SumCPar2 for a six **Basic Capacitor Cells** converter as function of p.



(c) SumCPar1 and SumCPar2 for a seven **Basic Capacitor Cells** converter as function of p.

Figure 2.8: SumCPar1 and SumCPar2 for different number of **Basic Capacitor Cells** converter.

C_{Par1_n-1} and C_{Par2_n-1} are short-circuited and have a voltage of $\frac{n-1}{n}.V_{DD}$. The rest of parasitic capacitances are in a similar situation but with the other fractions of the supply voltage ($\frac{n-2}{n}.V_{DD}$, $\frac{n-3}{n}.V_{DD}$, etc).

In Sub-Figure 2.9(b) the state of all the parasitic capacitances after the rotation process is shown. It can be seen that capacitors C_{Par1_n} and C_{Par2_n-1} have lost energy while the rest of the parasitic capacitances have gained energy. In steady state the mentioned energy lost by C_{Par1_n} and C_{Par2_n-1} is equal to the energy gained by the rest of the parasitic capacitances[7].

Equations (2.27) and (2.28) where derived assuming that the parasitic capacitances that lose energy during the rotation throw that energy to ground. Instead it is possible to make a redistribution of that charge to the parasitic capacitances that need to gain energy. Or, what is the same, the parasitic capacitances that need to lose energy can do it delivering energy to the parasitic capacitances that need to gain energy. For this the order in which the rotation sequence is performed is critical. Figure 2.10 shows the process.

Preparation For the Rotation Process

As capacitors of the ring ($C1$, $C2$,....Cn) are much larger than parasitic capacitances they can be considered as constant voltage source. Before the first step of the rotation it is needed that all the capacitors of the ring be floating and separate from the ring the capacitor whose parasitic capacitances will lose energy (Cn in Figure 2.10). So all switches $SWGnd$ must be kept opened during the rotation process and both $SwInter$ that connect Cn to the ring must be kept opened. This situation is shown in Sub-Figure 2.10(a).

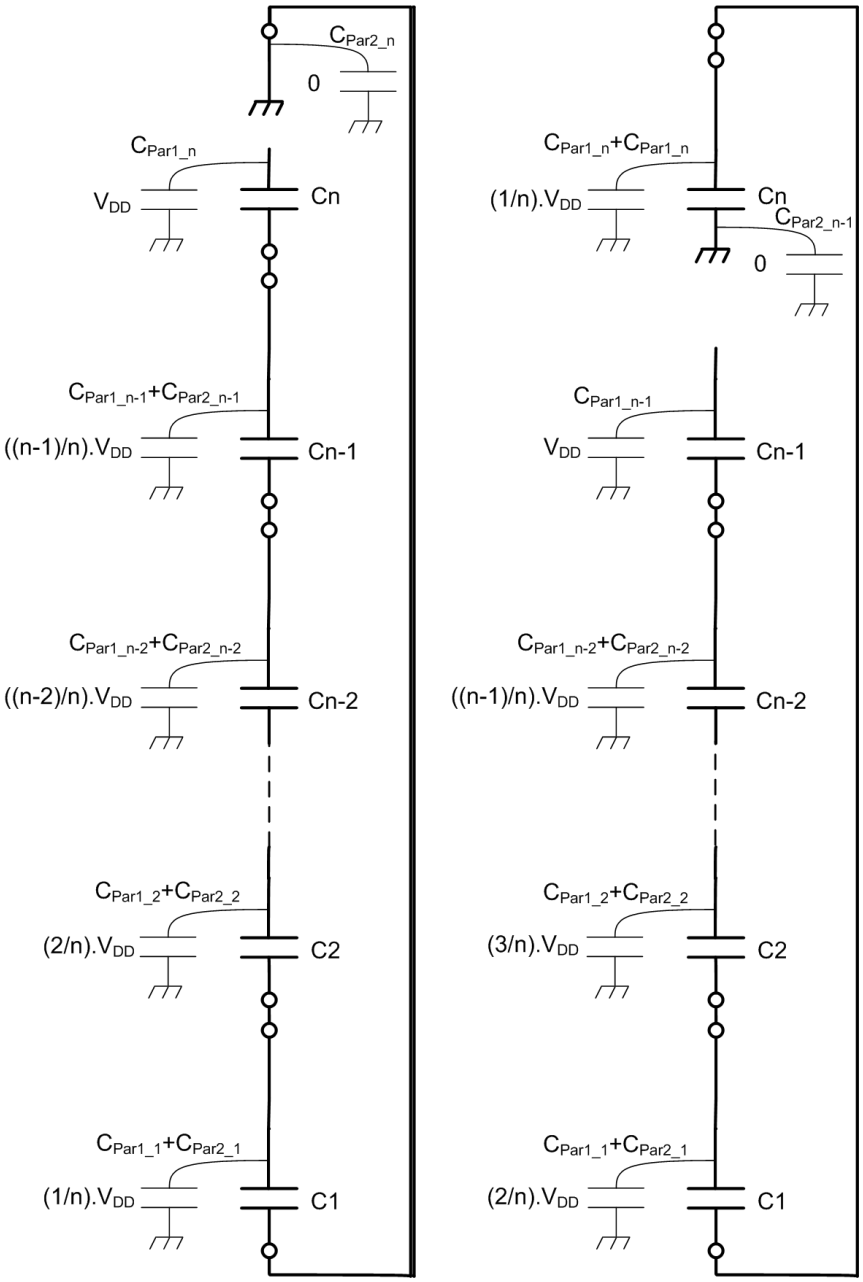
First Step in the Rotation Process

As energy lost in the energy transfer between two capacitors is proportional to the square of the difference in the initial voltage (Equation 1.3) the less is the difference the less is the energy lost. So the first step is to connect the parasitic capacitance C_{Par1_n} to the parasitic capacitance C_{Par1_n-1} that have less difference of voltage. That difference is $\frac{V_{DD}}{n}$. The mentioned situation is shown in Sub-Figure 2.10(b). As mentioned the capacitors of the ring can be considered as constant voltage sources, so if we consider only the variations in the parasitic capacitances the equivalent circuit is equal to the one shown in Figure 1.2, where $C1$ (the capacitor that delivers energy) is the parallel of C_{Par1_n} and C_{Par2_n-1} and $C2$ (the capacitor that takes energy) is the parallel of the rest of the parasitic capacitances.

If we define $C_{Par} = C_{Par1} + C_{Par2}$ then we have that: $C1 = C_{Par}$ and $C2 = (n-1).C_{Par}$. The energy lost in the first step is (using equation 1.3):

$$E_{Lost1} = \frac{C1.C2.\Delta V^2}{2.(C1+C2)} = \frac{C_{Par}.(n-1).C_{Par}.\Delta V^2}{2.(C_{Par}+(n-1).C_{Par})} = \frac{C_{Par}.(n-1).V_{DD}^2}{2.n^3} \tag{2.30}$$

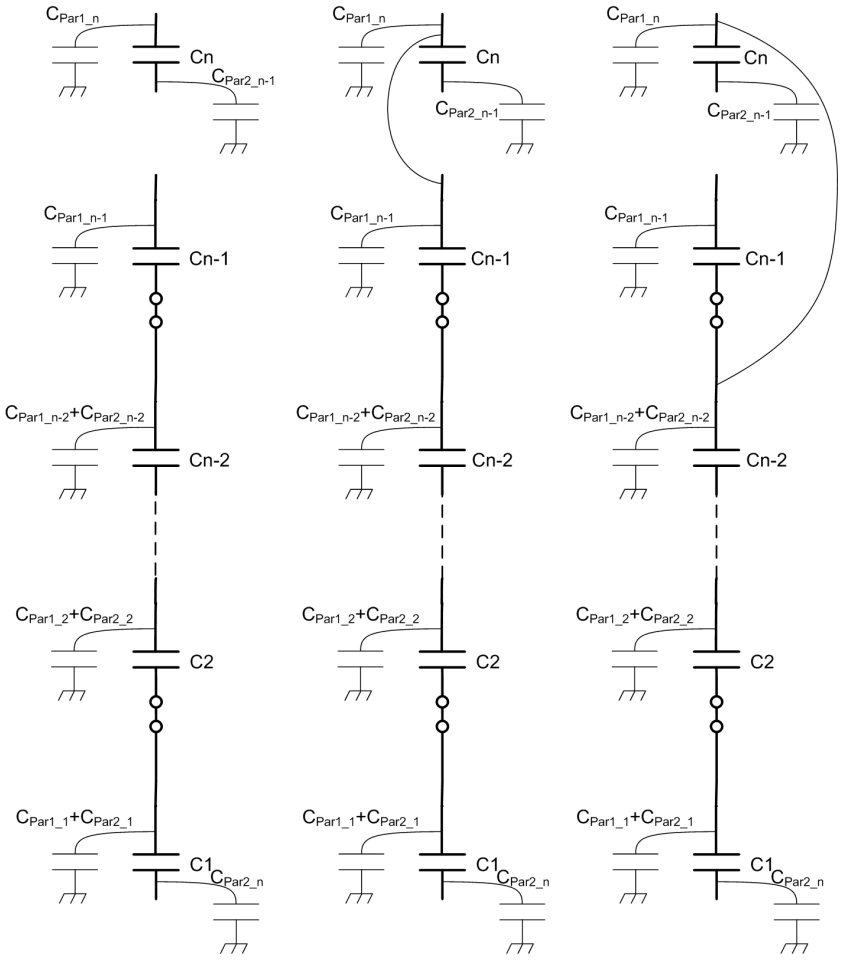
[7]This is because in steady-state the converter as a whole can't win energy.



(a) State before the rotation.

(b) Stare after the rotation.

Figure 2.9: State of the parasitic capacitances before and after the rotation.



(a) Cn capacitor separation. (b) First step. (c) Second step.

Figure 2.10: Rotation process.

Rest of Steps in the Rotation Process

The second step is to connect parasitic capacitance C_{Par1_n} to the parasitic capacitance C_{Par1_n-2} (see Sub-Figure 2.10(c)). The difference of voltage is again $\frac{V_{DD}}{n}$ and the equivalent circuit is the same as the first step. So the loss of energy is again the shown in equation (2.30).

This process is repeated until C_{Par1_n} is connected to the bottom plate of the capacitor $C1$ so the number of steps is n. Then the energy lost in the whole process is $n.E_{Lost1}$:

$$E_{LostRotation} = \frac{C_{Par}}{2}.V_{DD}^2.\frac{(n-1)}{n^2}$$

or

$$\boxed{\Delta E^*_{C_{Par}Total} = \frac{C_{Par1}}{2}.V_{DD}^2.\frac{(n-1)}{n^2} + \frac{C_{Par2}}{2}.V_{DD}^2.\frac{(n-1)}{n^2}} \tag{2.31}$$

with

$$\boxed{\Delta E^*_{C_{Par1}Total} = \frac{C_{Par1}}{2}.V_{DD}^2.\frac{(n-1)}{n^2}} \tag{2.32}$$

and

$$\boxed{\Delta E^*_{C_{Par2}Total} = \frac{C_{Par2}}{2}..V_{DD}^2.\frac{(n-1)}{n^2}} \tag{2.33}$$

Figure 2.11 shows an example of 5 **Basic Capacitor Cells** ring rotation. In Sub-Figure 2.11(a) the output voltage waveform and the top plate of the five capacitors of the ring are shown. Then in Sub-Figure 2.11(b) a zoom of the process of rotation (see the time axis) shows how the voltage of the capacitor $C5$ go down pulling up the rest of the capacitors.

2.5. Energy Saved with Improved Rotation Technique

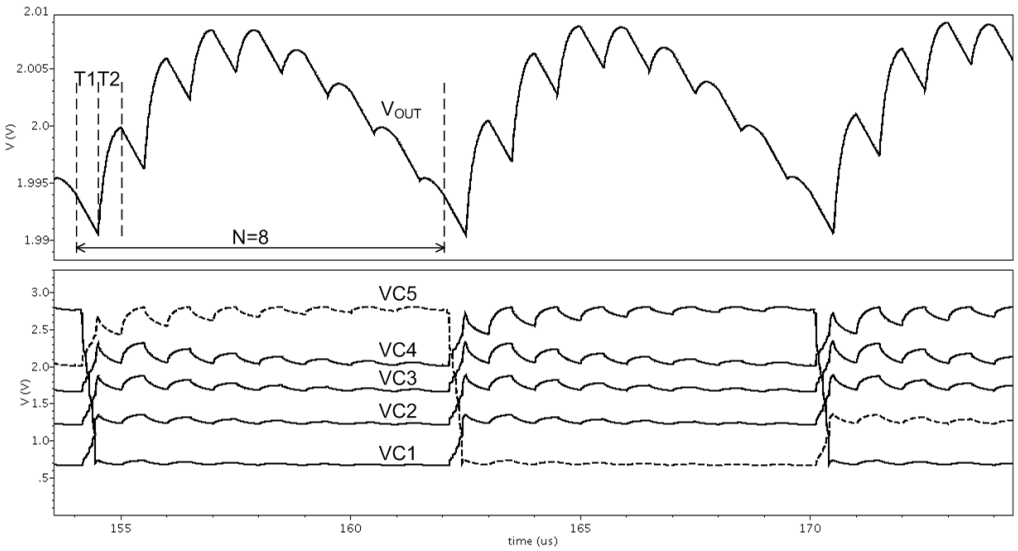
The energy saved with the technique can be computed comparing equations (2.29) and (2.31).In particular we can compare the contributions of C_{Par1} and C_{Par2} separately for each way of rotation. So we will see the expressions :

$$\frac{\Delta E^*_{C_{Par1}Total}}{\Delta E_{C_{Par1}Total}} = \frac{n-1}{n^2}.\frac{n^2}{n^2-1} = \frac{1}{n+1} \tag{2.34}$$

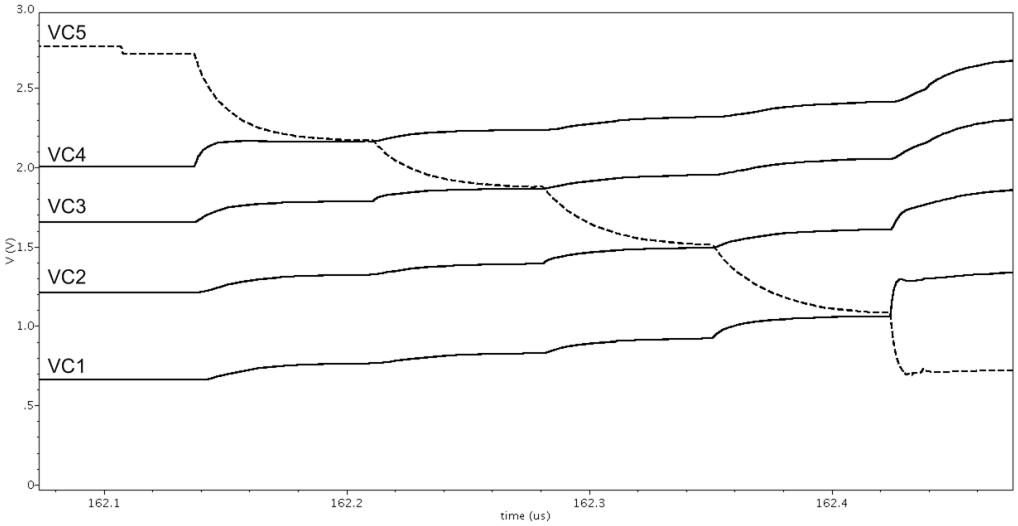
and

$$\frac{\Delta E^*_{C_{Par2}Total}}{\Delta E_{C_{Par2}Total}} = \frac{n-1}{n^2}.\left(\frac{n}{n-1}\right)^2 = \frac{1}{n-1} \tag{2.35}$$

The comparison is made in the table 2.1 as function of the number of capacitors of the ring (n). If we want to analyze the case of a five **Basic Capacitor Cells** converter,



(a) Output voltage and top plate voltages of the ring capacitors.



(b) Zoom of the top plate voltages in the rotation process.

Figure 2.11: Output and top plate voltages.

we must see the second row and it can be seen that the contribution of C_{Par1} decrease to $16{,}7\,\%$ in comparison with the original mechanism of rotation. In the case of the C_{Par2} the contribution decrease to $25\,\%$. As C_{Par1} (having the NWell-Substrate diode parasitic capacitance) is much bigger than C_{Par2} the main contribution to the parasitic capacitances losses comes from C_{Par1}. Thus the total power consumption in the parasitic capacitances will be reduced to close to $17\,\%$.

n	$\frac{1}{n+1}$	$\frac{1}{n-1}$
4	0.200	0.333
5	0.167	0.250
6	0.143	0.200
7	0.125	0.167

Table 2.1: Comparison of the two implementations of the rotation

2.6. The Control Logic

Figure 2.12 shows an schematic diagram of the logic used in the particular case of the designed converter. There is a "One Hot"[8] block that works as a pointer to the **Basic Capacitor Cell** in which the ring must be opened.

The block "Non Overlapping Clock Generator" generates from the main clock signal two non overlapped signals ($T1$ and $T2$) used to drive the gates of the switches $SwT1$ and $SwT2$.

The block "$SwT1$ Block" uses the signal $T1$ and the outputs of the different Flip Flops ($Q0...Q4$) to generate the five signals to drive the the gates of the switches $SwT1$. Basically it passes the signal $T1$ only to the **Basic Capacitor Cell** that is pointed by the "One Hot".

The block "$SwT2$ Block" uses the signal $T2$, the outputs of the different Flip Flops ($Q0...Q4$), and the signals $Sel0$ and $Sel1$ to generate the five signals to drive the gates of the switches $SwT2$. It works similar to the block "$SwT1$ Block" but passes the signal $T2$ only to the **Basic Capacitor Cell** that connects the ring to the output node. The signals $Sel0$ and $Sel1$ are used to select the conversion ratio as is shown in the table 2.2.

At last, the block "Rotation Block" implements the rotation of the ring. This happen when the block "Frequency Divider by Eight" enables the rotation. The signals $SwPar_{BCC0}...SwPar_{BCC0}$ are used to drive the switches that implement the parasitic capacitances losses reduction technique. These switches are connected as a "star" to the top plates of the different capacitors of the ring. The block uses a secondary signal clock with a fourteen times faster frequency than the main clock one. The block implements the rotation as described in the section 2.4 in the following order:

1. Open the switch $SwGnd$ that was closed and the switch $SwInter$ that will remain open after end of the rotation.

[8] A "One Hot block" is a ring of Flip Flops D that one of them has a one logic stored. Each clock edge the one logic is stored in the next Flip Flop of the ring.

Sel1	Sel0	Conv.Ratio
0	0	$1/5$
0	1	$2/5$
1	0	$3/5$
1	1	$4/5$

Table 2.2: Conversion ratio selection.

2. Implement the technique of reduction of parasitic capacitances losses.
3. Close the switch $SwInter$ that was opened before the start of the rotation process.
4. Close the switch $SwGnd$ that will remain closed after the end of the rotation.
5. Generates a signal used to shift the "One Hot"

2.7. Chapter Summary

Basic ideas were first presented and then the first problem to solve, that is the inability to return the charge to the point where the load is connected. This problem was solved implementing a mechanism of rotation that basically consist in changing the position of all the capacitors of the converter systematically.

For implementing the converter and the rotation a switches configuration was defined for each capacitor of the ring. The basic set "capacitor-switches configuration" was named **Basic Capacitor Cell** .

Then the implementation of the capacitors was presented. After this a charge transfer analysis was made.

The calculation of the parasitic capacitances consumption was made and, as this consumption is the most significant power loss, a technique to reduce it was proposed. The consumption of the parasitic capacitances was calculated again for the case when this technique is applied. Both results were compared having as a result that the proposed technique has a significant decrease in the parasitic capacitances losses.

At last, a brief analysis of the logic implementation was presented.

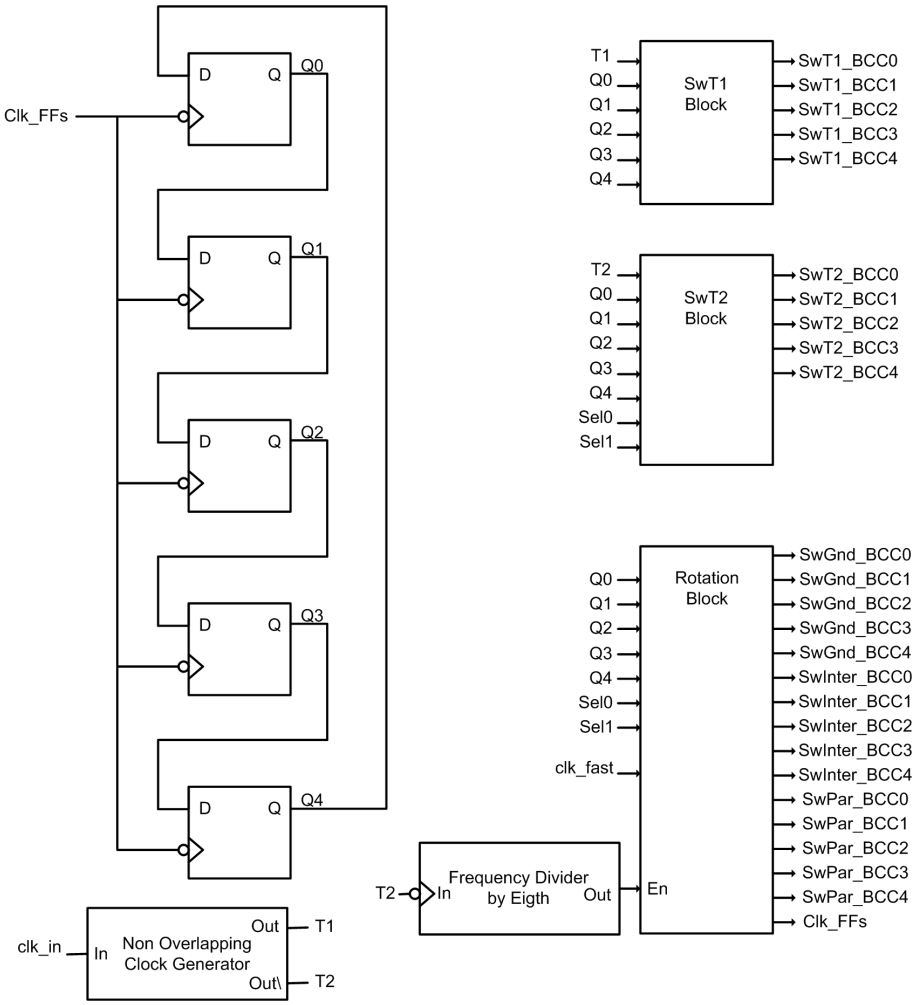


Figure 2.12: Block diagram of control logic.

CHAPTER 3

Numerical Model

Electrical simulations of medium-complexity circuits have long simulation times and are not suitable for design space exploration. In these cases it is helpful to have a numerical model that allows us to explore the design space automatically and at reasonable times. This chapter shows the numerical model developed for the converter with the purpose of exploring the design space.

A very important feature of the developed model is that it allows the designer to perform a design space exploration of any technology with little work. All the designer needs are some curves extracted from electrical simulation and some parameters of the technology.

First, the chapter shows the general considerations for the model, then the development of the model for the two phases. Finally, it shows how losses were modeled. In the appendix A the matlab files tree and the way to introduce the information required for other technologies are presented.

3.1. General Considerations for the Model

Since voltage-oriented models in circuits with non-linear capacitances can have cumulative errors as is described in [14], it is better to have a charge-oriented model, so this was the model used. Given that PMOS capacitors and switch resistances are non-linear the model developed is non-linear.

As mentioned, we used a charge-oriented model so the state variables are the charge of the capacitors. There are $n+1$ capacitors of which n make up the ring and the remaining one is C_L.

Figure 3.1 shows the converter for which the model was developed. Throughout this section a $\frac{m}{n}$ conversion ratio is considered with $0 < m < n$.

Equations used in the Matlab code are highlighted with double box.

3.1.1. Non-linear Capacitors

The non-linearity of the model comes from the fact that every capacitor is composed by a linear capacitor (poly1-poly2) in parallel with a non-linear capacitor (PMOS). So the equation that describes this combined device is:

$$Q = Q_{Linear} + Q_{PMOS} = C_{poly}.V + Q_{PMOS}(V) \tag{3.1}$$

Where $Q_{PMOS}(V)$ is described with a curve extracted from electrical simulations, so equation (3.1) must be solved numerically.

3.1.2. Switches Resistances

Resistance of CMOS switches are calculated from two curves(one for PMOS and one for NMOS transistors) extracted from electrical simulations. These curves have the resistance per width unit (in $\Omega.\mu m$)[1] as function of the source (drain) voltage. The gate voltage is supposed constant, equal to the supply voltage ($2{,}8V$) of the converter.

The curves were introduced in a matrix into a user defined function. This function, that uses linear interpolation needs the width of the transistor, the type of transistor ("n" or "p"), and source (drain) voltage. The function returns the resistance of the transistor.

To calculate the resistance of a complementary switch (one "n" transistor in parallel with a "p" transistor) it is necessary to calculate the two resistances separately and then calculate the parallel equivalent.

3.1.3. Representation in the State Space

If $\overrightarrow{Q}$ is the state vector composed by the charge of the $n+1$ capacitors, V_{DD} is the source voltage and I_L the load current, equation 3.2 shows the general model for the converter. Function f is different for each phase ($T1$ and $T2$) so we will develop two different functions which we will call $\overrightarrow{f}^{T1}$ and $\overrightarrow{f}^{T2}$.

$$\dot{\overrightarrow{Q}} = \begin{pmatrix} \dot{Q}_1 \\ \vdots \\ \dot{Q}_{m-1} \\ \dot{Q}_m \\ \dot{Q}_{m+1} \\ \vdots \\ \dot{Q}_n \\ \dot{Q}_L \end{pmatrix} = \begin{pmatrix} f_1(\overrightarrow{Q}, \overrightarrow{u}) \\ \vdots \\ f_{m-1}(\overrightarrow{Q}, \overrightarrow{u}) \\ f_m(\overrightarrow{Q}, \overrightarrow{u}) \\ f_{m+1}(\overrightarrow{Q}, \overrightarrow{u}) \\ \vdots \\ f_n(\overrightarrow{Q}, \overrightarrow{u}) \\ f_L(\overrightarrow{Q}, \overrightarrow{u}) \end{pmatrix} = \overrightarrow{f}(\overrightarrow{Q}, \overrightarrow{u}) \tag{3.2}$$

With:

$$\overrightarrow{u} = (V_{DD}, I_L)$$

[1] As all switches were designed with minimum length the only geometrical parameter considered is the width.

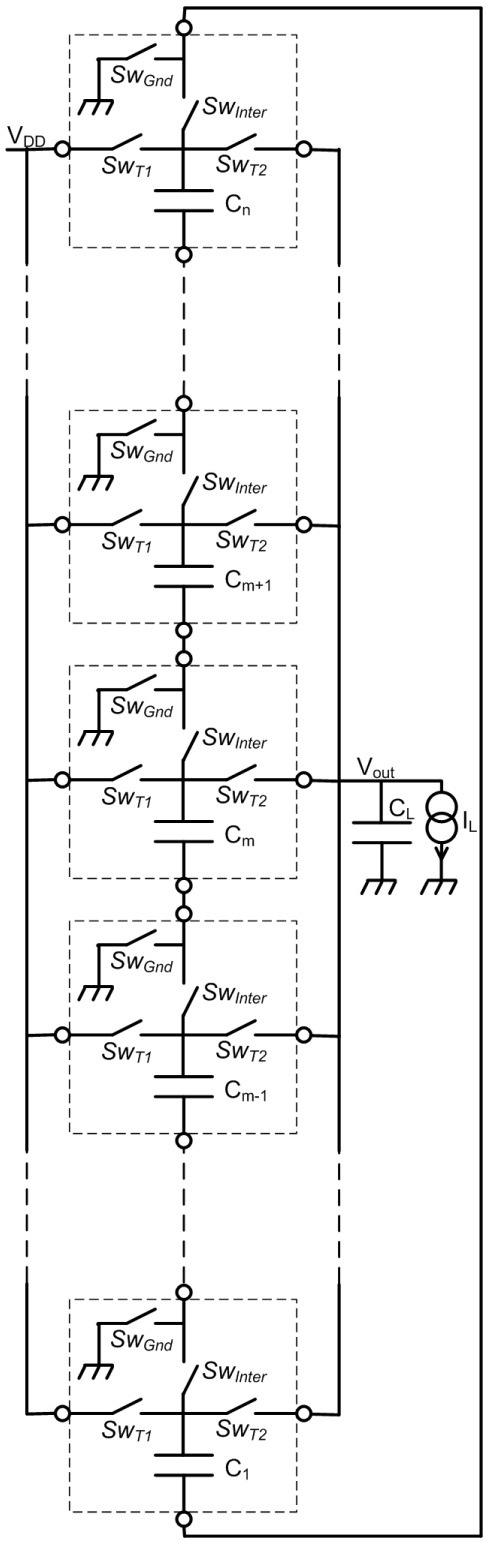


Figure 3.1: N **Basic Capacitor Cells** Converter

To develop a numerical model we must make the following approximation:

$$\dot{\overrightarrow{Q}} \simeq \frac{\Delta\overrightarrow{Q}}{\Delta t} \tag{3.3}$$

Where Δt is a differential time. So if we want to solve the differential equation in each phase in $NumSteps$ steps we have the following equations $\Delta t = \frac{T1}{NumSteps}$ or $\Delta t = \frac{T2}{NumSteps}$ that are equal in our case because $T1 = T2 = \frac{T_{SW}}{2}$.

$$\Delta\overrightarrow{Q} = \overrightarrow{Q}(t + \Delta t) - \overrightarrow{Q}(t) \tag{3.4}$$

So from equations (3.2), (3.3) and (3.4) we have that:

$$\overrightarrow{Q}(t + \Delta t) \simeq \overrightarrow{Q}(t) + \overrightarrow{f}(\overrightarrow{Q}, \overrightarrow{u}).\Delta t$$

Or for numerical models:

$$\overrightarrow{Q}(k + 1) = \overrightarrow{Q}(k) + \overrightarrow{f}(\overrightarrow{V}(\overrightarrow{Q}(k)), u).\Delta t$$

With:

$$\overrightarrow{V}(\overrightarrow{Q}) = \begin{pmatrix} V_n(Q_1) \\ \vdots \\ V_{m+1}(Q_{m-1}) \\ V_m(Q_m) \\ V_{m-1}(Q_{m+1}) \\ \vdots \\ V_1(Q_n) \\ V_{C_L}(Q_{C_L}) \end{pmatrix}$$

Where $V_k(Q_k) \quad \forall k = 1 : n$ and $V_{C_L}(Q_{C_L})$ means the dependence of the voltage of the capacitor with its own charge. The dependence of f with Q was written in this way because it is more convenient for the equations developed in next sections.

So

$$\begin{pmatrix} Q_1(k+1) \\ \vdots \\ Q_{m-1}(k+1) \\ Q_m(k+1) \\ Q_{m+1}(k+1) \\ \vdots \\ Q_n(k+1) \\ Q_{C_L}(k+1) \end{pmatrix} = \begin{pmatrix} Q_1(k) \\ \vdots \\ Q_{m-1}(k) \\ Q_m(k) \\ Q_{m+1}(k) \\ \vdots \\ Q_n(k) \\ Q_{C_L}(k) \end{pmatrix} + \begin{pmatrix} f_1(\overrightarrow{V}(\overrightarrow{Q}(k)), \overrightarrow{u}) \\ \vdots \\ f_{m-1}(\overrightarrow{V}(\overrightarrow{Q}(k)), \overrightarrow{u}) \\ f_m(\overrightarrow{V}(\overrightarrow{Q}(k)), \overrightarrow{u}) \\ f_{m+1}(\overrightarrow{V}(\overrightarrow{Q}(k)), \overrightarrow{u}) \\ \vdots \\ f_n(\overrightarrow{V}(\overrightarrow{Q}(k)), \overrightarrow{u}) \\ f_{C_L}(\overrightarrow{V}(\overrightarrow{Q}(k)), \overrightarrow{u}) \end{pmatrix} \Delta t \tag{3.5}$$

The output for the two phases is given by:

$$\boxed{V_{OUT} = V_{C_L}(Q_{C_L})} \tag{3.6}$$

Here it is important to notice that despite in all the equations the supply voltage is considered as a parameter that can be changed, this change must take into account the data extracted from electrical simulations. In particular the switches resistances and the buffers consumption are extracted from electrical simulations for a particular supply voltage, so it is needed to make a different extraction for each supply voltage value. Look appendix A for more details.

3.2. Phase T1

The equivalent circuit for the phase $T1$ is shown in figure 3.2(a) so we have the next equations:

$$I_{Cn} = \ldots = I_{Cm+1} = I_{Cm} = I_{Cm-1} = \ldots = I_{C1} = \dot{Q_k}; \quad \forall k = 1:n \tag{3.7}$$

$$\dot{Q_{CL}} = I_{CL} = -I_L \tag{3.8}$$

$$V_{DD} = \sum_{r=1}^{n} V_{C_r}(Q_r) + \sum_{z=1}^{n-1} V_{R_z} + V_{R_{SwGnd}} + V_{R_{SwT1}} \tag{3.9}$$

If we make the following definition:

$$R_{T1} = \sum_{z=1}^{n-1} R_z + R_{SwGnd} + R_{SwT1} \tag{3.10}$$

From equations (3.7), (3.9), (3.10) and the Ohm law we have that:

$$V_{DD} = \sum_{r=1}^{n} V_{C_r}(Q_r) + R_{T1}.\dot{Q_k}; \quad \forall k = 1:n \tag{3.11}$$

So

$$\dot{Q_k} = \left[V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r) \right] . \frac{1}{R_{T1}}; \quad \forall k = 1:n \tag{3.12}$$

Using equations (3.8) and (3.12) we have the function $\overrightarrow{f}(\overrightarrow{Q}, \overrightarrow{u})$ in the phase $T1$:

$$\overrightarrow{f}^{T1}(\overrightarrow{Q}, \overrightarrow{u}) = \begin{pmatrix} [V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r)] . \frac{1}{R_{T1}} \\ \vdots \\ [V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r)] . \frac{1}{R_{T1}} \\ [V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r)] . \frac{1}{R_{T1}} \\ [V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r)] . \frac{1}{R_{T1}} \\ \vdots \\ [V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r)] . \frac{1}{R_{T1}} \\ -I_L \end{pmatrix} \tag{3.13}$$

Therefore the equation to use in the numerical model during the phase $T1$ is:

$$\begin{pmatrix} Q_1^{T1}(k+1) \\ \vdots \\ Q_{m-1}^{T1}(k+1) \\ Q_m^{T1}(k+1) \\ Q_{m+1}^{T1}(k+1) \\ \vdots \\ Q_n^{T1}(k+1) \\ Q_{C_L}^{T1}(k+1) \end{pmatrix} = \begin{pmatrix} Q_1^{T1}(k) \\ \vdots \\ Q_{m-1}^{T1}(k) \\ Q_m^{T1}(k) \\ Q_{m+1}^{T1}(k) \\ \vdots \\ Q_n^{T1}(k) \\ Q_{C_L}^{T1}(k) \end{pmatrix} + \begin{pmatrix} \left[V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r^{T1}(k))\right] \cdot \frac{1}{R_{T1}} \\ \vdots \\ \left[V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r^{T1}(k))\right] \cdot \frac{1}{R_{T1}} \\ \left[V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r^{T1}(k))\right] \cdot \frac{1}{R_{T1}} \\ \left[V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r^{T1}(k))\right] \cdot \frac{1}{R_{T1}} \\ \vdots \\ \left[V_{DD} - \sum_{r=1}^{n} V_{C_r}(Q_r^{T1}(k))\right] \cdot \frac{1}{R_{T1}} \\ -I_L \end{pmatrix} .\Delta t \tag{3.14}$$

3.3. Phase T2

The equivalent circuit for the phase $T2$ is shown in Figure 3.2(b) so we have the next equations:

$$\begin{array}{c} I_{Cm} = I_{Cm-1} = \ldots = I_{C1} = \dot{Q}_k; \quad \forall k = 1:m \\ 0 = I_{Cn} = \ldots = I_{Cm+1} = \dot{Q}_k; \quad \forall k = m+1:n \end{array} \tag{3.15}$$

$$\dot{Q}_{CL} = I_{CL} = -(I_L + \dot{Q}_k); \quad \forall k = 1:m \tag{3.16}$$

$$V_{OUT} = \sum_{r=1}^{m} V_{C_r}(Q_r) + \sum_{z=1}^{m-1} V_{R_z} + V_{R_{SwGnd}} + V_{R_{SwT2}} \tag{3.17}$$

If now the make the following definition:

$$R_{T2} = \sum_{z=1}^{m-1} R_z + R_{SwGnd} + R_{SwT2} \tag{3.18}$$

From equations (3.6), (3.15), (3.17), (3.18) and the Ohm law we have that:

$$V_{C_L}(Q_{C_L}) = \sum_{r=1}^{m} V_{C_r}(Q_r) + R_{T2}.\dot{Q}_k; \quad \forall k = 1:m \tag{3.19}$$

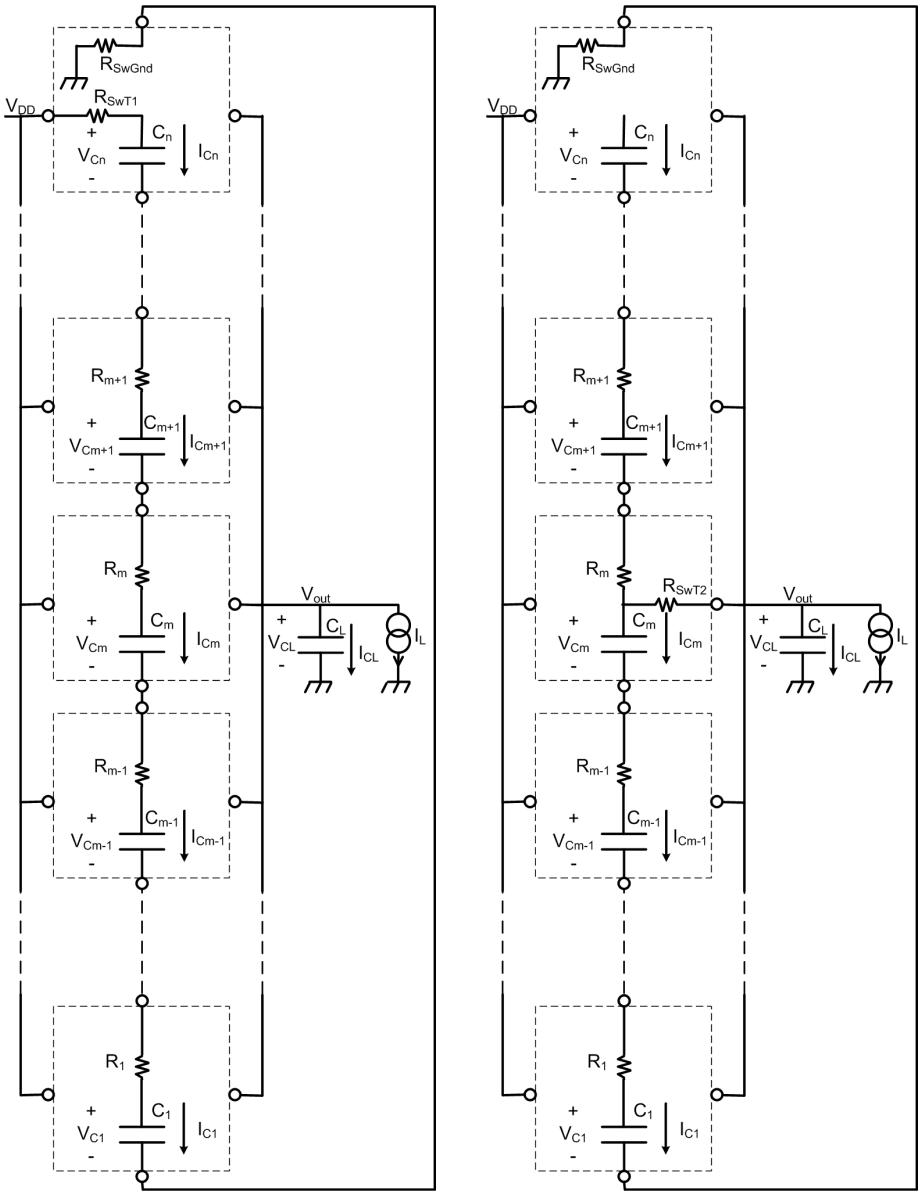
and

$$\dot{Q}_k = \left[V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)\right] . \frac{1}{R_{T2}} \quad \forall k = 1:m \tag{3.20}$$

So from equations (3.15) and (3.20) we have that

$$\dot{Q}_k = \begin{cases} \left[V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)\right] \cdot \frac{1}{R_{T2}} & \forall k = 1:m \\ 0 & \forall k = m+1:n \end{cases} \tag{3.21}$$

Then form equations (3.16) and (3.20):



(a) T1 phase equivalent circuit. (b) T2 phase equivalent circuit.

Figure 3.2: N **Basic Capacitor Cells** ring circuits for numerical model

$$\dot{Q}_{CL} = \left[\sum_{r=1}^{m} V_{C_r}(Q_r) - V_{C_L}(Q_{C_L})\right] \cdot \frac{1}{R_{T2}} - I_L \tag{3.22}$$

Using equations (3.21) and (3.22) we have the function $\overrightarrow{f}(\overrightarrow{Q}, \overrightarrow{u})$ in the phase $T2$:

$$\overrightarrow{f}^{T2}(\overrightarrow{Q}, \overrightarrow{u}) = \begin{pmatrix} [V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)] \cdot \frac{1}{R_{T2}} \\ \vdots \\ [V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)] \cdot \frac{1}{R_{T2}} \\ [V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)] \cdot \frac{1}{R_{T2}} \\ 0 \\ \vdots \\ 0 \\ [\sum_{r=1}^{m} V_{C_r}(Q_r) - V_{C_L}(Q_{C_L})] \cdot \frac{1}{R_{T2}} - I_L \end{pmatrix} \tag{3.23}$$

Then

$$\boxed{\begin{pmatrix} Q_1^{T2}(k+1) \\ \vdots \\ Q_{m-1}^{T2}(k+1) \\ Q_m^{T2}(k+1) \\ Q_{m+1}^{T2}(k+1) \\ \vdots \\ Q_n^{T2}(k+1) \\ Q_{C_L}^{T2}(k+1) \end{pmatrix} = \begin{pmatrix} Q_1^{T2}(k) \\ \vdots \\ Q_{m-1}^{T2}(k) \\ Q_m^{T2}(k) \\ Q_{m+1}^{T2}(k) \\ \vdots \\ Q_n^{T2}(k) \\ Q_{C_L}^{T2}(k) \end{pmatrix} + \begin{pmatrix} [V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)] \cdot \frac{1}{R_{T2}} \\ \vdots \\ [V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)] \cdot \frac{1}{R_{T2}} \\ [V_{C_L}(Q_{C_L}) - \sum_{r=1}^{m} V_{C_r}(Q_r)] \cdot \frac{1}{R_{T2}} \\ 0 \\ \vdots \\ 0 \\ [\sum_{r=1}^{m} V_{C_r}(Q_r) - V_{C_L}(Q_{C_L})] \cdot \frac{1}{R_{T2}} - I_L \end{pmatrix} .\Delta t} \tag{3.24}$$

3.4. Energy Losses

There are essentially four types of energy losses that were presented in section 1.2. This section describes them and shows how they were estimated.

3.4.1. Parasitic Capacitances Losses

As derived in section 2.4, the equation (2.31) describes the losses in charging and discharging the parasitic capacitances. So this one is the equation used.

3.4.2. Gate-drive Losses

To calculate Gate-drive losses two curves extracted from electrical simulations were used, one for “n” transistors and the second one for “p” transistors. These curves have the switching losses per width unit (in $Joules/\mu m$)[2] as function of the source

[2] As all switches were designed with minimum length the only geometrical parameter considered is the width.

(drain) voltage.

The curves were introduced in a matrix into a user defined function. This function needs the width of the transistors of the switch (the “n” and the “p”) and source (drain) voltage. It returns the energy consumed in a on-off cycle of the switch.

3.4.3. Conduction Losses

There are two equivalent resistors (see equations (3.10) and (3.18)) that dissipate energy, each one associated with one phase of the converter. As the equations (3.14) and (3.24) were solved step by step, the resistance was calculated in every step to take into account its dependence on system state. So to calculate the dissipated energy we must use for each step the equation:

$$\Delta E_{R_{Ti}}(k) = R_{Ti}(k).i^2_{R_{Ti}}(k).\Delta t \quad i = 1:2 \tag{3.25}$$

Then, the energy dissipated in one period of switching ($T1 + T2$) is:

$$E^{T1+T2}_{ResLoss} = \sum_{k=i}^{NumSteps} \left(R_{T1}(k).i^2_{R_{T1}}(k).\Delta t\right) + \sum_{k=i}^{NumSteps} \left(R_{T2}(k).i^2_{R_{T2}}(k).\Delta t\right) \tag{3.26}$$

3.4.4. Digital and Analog Control Circuits Losses

The Digital Circuits losses are considered in two different ways. The first one is the logic consumption that is needed to implemente the two phases of the converter. The second one is the logic consumption to implement the rotation process. It is needed to have these two values to calculate the performance of the circuit.

After each execution of the phases $T1$ and $T2$ the logic consumption used to implement these phases is added in a variable that accumulate the total logic losses. The same happens when a rotation is performed with the logic consumption used to implement the rotation.

As mentioned in the introduction, analog circuit losses are considered into the logic losses. The bias current considered is $100nA$ so the energy si calculated as:

$$E_{Analog} = V_{DD}.I_{BIAS}.(t_f - t_i) \tag{3.27}$$

Where I_{BIAS} is the total bias current of the analog circuits, and t_i and t_f are the initial and final time where the power was integrated.

3.5. How the Model Works

For the model we have two kind of magnitudes: those associated to the dynamic of charging and discharging capacitors that have variation with continuous time, and those associated to events such as closing and opening switches that are associated to discrete times. This section describe all the considered magnitudes and shows how the

model integrates them to calculate the performance of the circuit. It exists in the model the possibility to calculate the performance in steady state or including the transient.

3.5.1. Magnitudes That Change With Each Time Step

Charge

Q is the vector that contains the charge of the $n + 1$ capacitors of the converter (see equation (3.2)). From this magnitude are obtained voltage and current. Voltage is calculated from equation (3.1) and current deriving in time.

Energy Taken from Supply Voltage

As the energy taken from the supply voltage is given by equation (2.11), it is needed to calculate during $T1$ the charge taken from the source. During $T2$ no current is taken by the core of the converter from the supply voltage (the analog circuits, gate drive and the logic take energy from the supply voltage but these losses are considered in a different way). After $T1$ the energy calculated is added to the cumulative energy value taken from the source.

Resistances

To have an accurate transient and dissipated energy in resistors it is necessary to calculate the resistances R_{T1} and R_{T2} dynamically so are calculated every Δt times during $T1$ and $T2$ respectively.

Energy Dissipated in Resistances

The energy dissipated in $RT1$ and $RT2$ is calculated integrating numerically during $T1$ and $T2$ respectively using equation 3.26. After each phase the energy calculated is added to the cumulative energy value dissipated in the resistances.

3.5.2. Magnitudes That Change With Events

Energy Dissipated in Switches $SWT1$ and $SWT2$

After the execution of $T1$ the energy consumed in the cycle of opening and closing this switch is calculated. Then this value is added to a variable that stores the accumulated wasted energy.Exactly the same happens with $SWT2$.

Energy Dissipated in Switches Associated to Rotation ($SWInt$ y $SWGnd$)

After a rotation the energy consumed in the cycle of opening and closing the switches $SWInter$ and $SWGnd$ is calculated. Then this value is added to a variable that stores the accumulated wasted energy.

Energy Dissipated Charging Parasitic Capacitances in the Rotation

After a rotation the energy consumed in charging and discharging parasitic capacitances is calculated. Then, this value is added to a variable that stores the accumulated wasted energy.

```
while iterate
    for i = 1:NumRotations
        for k = 1:NumPeriods
            for j = 1:NumSteps % (T1 simulation)
                RT1 calculation
                Differential charge calculus and concatenation
                Addition of supply voltage energy
                Addition of RT1 energy disipation
                Energy stored in capacitors
            end
            Addition of SWT1 switching
            for m = 1:NumSteps % (T2 simulation)
                RT2 calculation
                Differential charge calculus and concatenation
                Addition of RT2 energy disipation
                Energy stored in capacitors
            end
            Addition of SWT2 switching
        end
        Rotation Implementation
        Addition of Rotation Energy
        Save state
    end
    mean comparison
end
```

Figure 3.3: Model Pseudo Code

Energy Dissipated In Control Circuits

After the execution of $T1$ and $T2$ the energy consumed by the logic in this cycle is added to a variable that stores the accumulated wasted energy. After the execution of a rotation the energy consumed by the logic in this process is added to the same variable.

The energy needed to supply the analog circuits is calculated at the end of the simulation and added to the accumulated value too.

3.5.3. Model Pseudo Code

Figure 3.3 shows the pseudo code used, where it can be seen that there is a **while** statement that eliminates the transient in an iterating process. Inside the **while** statement there is a **for** instruction that runs $NumRotations$ times, that is the number of rotations of the ring that wants to be included in the simulation. Then, there is a **for** statement that runs $NumPeriods$ which is the number of periods ($T1 + T2$) that the simulator runs before making the rotation of the ring. At last there are two **for** statements that run $NumSteps$ times, which implement $T1$ and $T2$.

In the last rotation the state is saved in order to be used to start the next simulation, if necessary. At the end of the **while** (simulation has been completed) the temporal mean of the charge in capacitor C_L is compared with the same value of the previous simulation. If there is a significant difference it is because the transient has not been removed so the simulation starts again but in the state saved in the last rotation. Thus, the simulator simulates the converter as many times as necessary to remove the transient and calculate the performance in steady-state. When the comparison of the temporal mean of the charge of C_L of two consecutive simulations is negligible, the transient has been removed so it is no longer necessary to continue iterating.

Inside the **for** statements that implements step by step the phases $T1$ and $T2$ the associated resistance is calculated and then the charge variations using equations (3.14) and (3.24).

3.6. Comparison with Electrical Simulations

In order to know how accurate the model is, a comparison between electrical and numerical simulations is made in this section. These simulations were made for the converter designed with a conversion ratio of $\frac{4}{5}$, a current load of $50\mu A$, a switching frequency of $500kHz$ and $N = 8$. The energy was computed integrating the power in a period of $80\mu s$ in steady-state. The comparison between both simulations is shown in the Table 3.1 where the following parameters are shown :

- $V_{Ripple}(mV)$ - Ripple voltage.
- $E_L(J)$ - Energy delivered to the load.
- $E_{CparCond}(J)$ - Energy lost in conduction and parasitic capacitances losses.
- $E_{Log}(J)$ - Energy lost in the logic.
- $E_{Sw}(J)$ - Energy lost in gate driving
- eff ($\%$) - Efficiency ($\frac{E_L}{E_L+E_{CparCond}+E_{Log}(J)+E_{Sw}}$).

Here it is important to highlight that the parasitic capacitances and conduction losses are presented in a single variable. This is because although both losses have very different origins, the two are evidenced in the same way, namely power dissipation in the switches, so they are difficult to separate in electrical simulations.

In the table it can be seen that the differences between both simulations are small. In particular the efficiency has a difference of $1\,\%$.

On the other hand, while the numerical model has a low accuracy when the efficiency is low (less than $20\,\%$) the accuracy is very good for all the efficiency levels of interest for the designer. So the model is very good for making a first order analysis and taking decisions shown in the next section.

Figures 3.4 shows the output voltage waveforms for two rotations of the ring. While the simulation is made in a time window of $80\mu A$ what is equivalent to eight rotations of the ring, in the Figure just two rotations are shown.

Parameter	$V_{Ripple}(mV)$	$E_L(J)$	$E_{CparCond}(J)$	$E_{Log}(J)$	$E_{Sw}(J)$	eff $(\%)$
Electrical Sim.	21	8.13e-9	1.71e-9	5.33e-10	4.12e-10	77.85
Numerical Sim.	17	7.85e-9	1.51e-9	5.28e-10	3.00e-10	77.00

Table 3.1: Comparison between electrical and numerical simulations

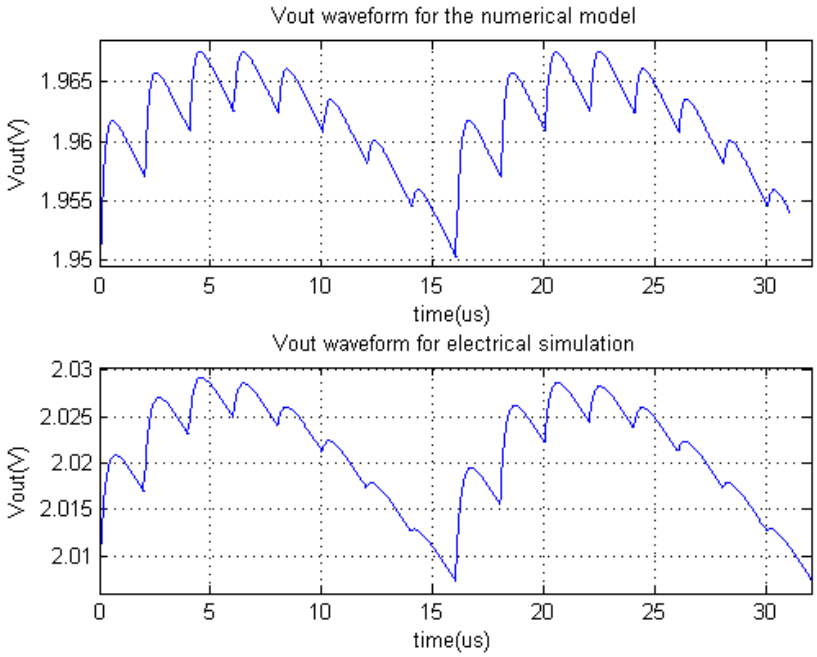


Figure 3.4: V_{OUT} waveforms for numerical and electrical simulations.

3.7. Design Space Exploration for Optimum N Selection

The number of periods between consecutive rotations of the ring (N) impacts mainly in two of the energy losses of the converter The larger the value of N is the less the output average voltage for a given conversion ratio and a given load current is. As the conduction loss depends on the difference between the real output voltage and the ideal output voltage, the bigger is the value of N the bigger are the conduction losses. So to minimize conduction losses we must minimize the value of N. On the other hand, the larger the value of N is the less the parasitic capacitances losses are, so there is a trade-off between conduction and parasitic capacitances losses that can be managed with the value of N.

To know which is the best value of N for the converter designed, a design space exploration was made with variations in the load current, conversion ratio, switching frequency and N. To decide the best value of N, the analysis is made for a load current

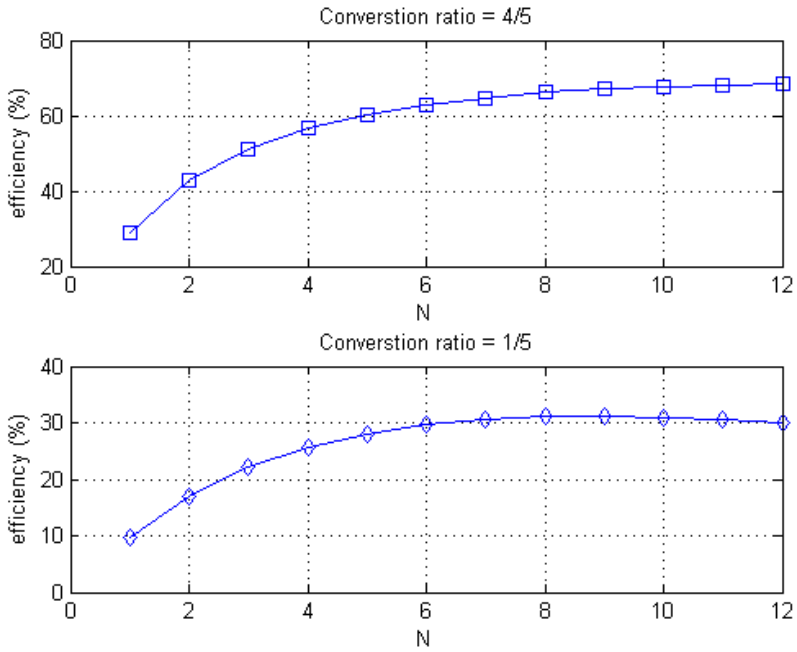


Figure 3.5: Efficiency as a function of $N_{@I_L=100\mu A}$.

of $100\mu A$ because it is the largest current for which the converter was designed. In the chapter where the feedback loop is analyzed it will be seen that for minor currents the efficiency will keep essentially constant.

Figure 3.5[3] shows the efficiency for this current load for the cases of conversion ratio of $4/5$ and $1/5$ (the largest and the smallest conversion ratios). In the case of conversion ratio of $4/5$ it can be seen that the peak of efficiency is achieved for a value of N higher than the one shown in the figure. On the other hand, for the case of conversion ratio of $1/5$ the peak of efficiency is achieved in the case $N = 9$. In digital circuits having frequencies derived from the main clock is much easier when this derivation is made by powers of two. So $N = 8$ is the best choice for the designed converter because it has an efficiency that is near the peak in the case of conversion ratio of $1/5$ and it has a very good efficiency in the caso of $4/5$. So the case $N = 8$ is the one chosen.

As this space design exploration was made before the implementation of the technique to decrease the parasitic capacitances losses, the efficiency values are significantly lower than in the final design.

[3]Although in the graphs a continuous line can be seen the only purpose that it has is to shows the trend. The only points that have a real sense are those for which $N \in \mathbb{N}$.

CHAPTER 4

Proposed Control Scheme

In this chapter a feedback loop is proposed. This control mechanism will allow us to achieve the two main aims of a **DC-DC Converter** . The most basic aim of a **DC-DC Converter** is to supply a constant voltage to the load. Another important aim is to have a constant efficiency independent of the current load.

If we are looking for applications such as supply of micro-controllers and use the technique **Dynamic Voltage Scaling** to minimize the power consumption without having a negative impact in the performance of the circuit, a constant efficiency is needed. If for example the converter has a good efficiency for high currents (η_{Active}) but a bad efficiency for low currents (η_{Sleep}), the real average efficiency of the converter in the application will be good or bad depending of the relationship of the duration between sleep and active modes (T_{Sleep} and T_{Active}) and the power consumption in both modes (P_{Sleep} and P_{Active}). Equation (4.1) shows the expression of the combined efficiency. So having an efficiency independent of the load power (or equivalently independent of the load current) is necessary to avoid having an efficiency that depends on the application.

$$\eta_{Comb} = \frac{P_{Active}.T_{Active} + P_{Sleep}.T_{Sleep}}{\frac{P_{Active}.T_{Active}}{\eta_{Active}} + \frac{P_{Sleep}.T_{Sleep}}{\eta_{Sleep}}} \tag{4.1}$$

Thinking in the more basic aim that is having a constant output voltage, Figure 1.6 shows an equivalent circuit for a **Switched Capacitor Converter** . To have a constant output voltage it is necessary to have a constant voltage drop in the output resistance R_{OUT} for all load currents. As stated in section 1.2.3 the output resistance has a component independent of the switching frequency (R_{FSL}) and another that varies inversely proportional to it (R_{SSL}). To know which one is the best mode for working (fast or slow switching limit) we must analyze the implications of each one.

Fast Switching Limit (FSL) mode implies that each phase has a very short duration (much less than the different time constants (τ) of the different topologies) and this

will have a negative impact in the efficiency because the logic, parasitic capacitances and gate-drive losses will be very high. Furthermore, in this mode the output resistance is independent of any parameter that can be controlled in real time[1] so regulation of the output voltage is very difficult because the drop voltage in the output resistance is dependent of the current load. So working in this mode must be avoided.

On the other side, Slow Switching Limit (SSL) implies that each phase has a very long time duration (much longer than the different time constants (τ) of the different topologies), enough to consider that the voltage waveforms are square. In this case the time to transfer energy between capacitors or between the supply voltage and the capacitors is enough to consider that capacitors achieve the steady-state. So it is clear that this mode is more appropriate because it allows to transfer energy with a minimum of energy losses in logic, gate drive and parasitic capacitances. Furthermore, in this mode the output resistance has an inversely proportional dependence with the switching frequency that is a parameter that can be changed in real time.

However, it is important to note that the energy transferred to a capacitor is independent of the transient and only depends of the initial and final conditions. So if we have phase durations for example of ten time constants ($\tau = T1/10$) the voltage achieved by the capacitors will be in the $99{,}995\,\%$ of the asymptotic final value. But if we decrease the switches width to half of the original case, the new time constants are multiplied by two($\tau^* = T1/5$), so the phases have a time duration of approximately $5.\tau^*$ and the final voltage will be in the $99{,}326\,\%$ of the asymptotic final value what is essentially the same. But if we consider the gate drive losses the second case has just the $50\,\%$ of consumption than in the first case. So the optimum point to design a **Switched Capacitor Converter** must be in the transition where none of the two modes are valid.

As stated at the beginning of this chapter, a feedback loop will be proposed. The proposed one consists in changing the switching frequency as a function of the load current. So to achieve the maximum target current delivered to the load ($100\mu A$) the design is made in the "optimum" point for this case. When the current load decreases the frequency will decrease and the operation mode will be going into the SSL. We will demonstrate that this feedback loop will allow us to achieve a constant efficiency. However it can be improved if we make smaller the switches when the frequency becomes lower, or equivalently if we use switches with a width proportional to the load current. This improvement was not implemented but this optimization will be analyzed in section 6.1.

4.1. Feedback Loop Analysis

As mentioned in the previos paragraph, the converter will work in the SSL and in the limit where no one of the two asymptotic limits are valid, the SSL resistance is dominant. So for us the output resistance in the Figure 1.6 will be inversely proportional to the switching frequency. If this is the case the drop voltage in the resistance is $V_{Drop} = R_{OUT}.I_L$ or $V_{Drop} = \frac{K_{SSL}}{f_{Sw}}.I_L$. So it is clear that to have an output voltage

[1] This resistance just depends on switch resistances and the topologies of the converter.

independent of the current load it is necessary to have a switching frequency proportional to the current load. Thus if $f_{Sw} = K_{I_L}.I_L$ the voltage drop in the output resistance becomes constant with the value $V_{Drop} = \frac{K_{SSL}}{K_{I_L}}$. It is clear that when the load current (and as consequence f_{Sw}) is increasing and $R(f_{SSL})$ becomes negligible in comparison with R_{FSL} the output voltage will start to decrease independent of the switching frequency because the drop voltage in the resistance would be $V_{Drop} = R_{FSL}.I_L$. Or equivalently, the converter is working in FSL.

To analyze the effect in the efficiency of having a switching frequency that has a linear dependence with the current load, the efficiency of a general converter can be written from equations (1.5) and (1.6) as:

$$\eta = \frac{E_{out}}{E_{in}} = \frac{E_{load}}{E_{load} + E_{cond} + E_{gates} + E_{par} + E_{logic}} \tag{4.2}$$

Here we have that all the losses have a linear dependence with the switching frequency with the exception of the logic losses that can have both a frequency dependence factor and a constant factor due to the bias current of analog circuits such as amplifiers or comparators. In the case of the energy delivered to the load if we consider that the output voltage is approximately constant, it can be written as $E_{Load} = V_{OUT}.I_L.\Delta t$ or $E_{load} = K_{Load}.f_{Sw}$ where Δt is the period of time where the power was integrated and $K_{Load} = \frac{V_{OUT}.\Delta t}{K_{I_L}}$. And the equation (4.2) can be written as:

$$\eta = \frac{K_{Load}.f_{Sw}}{K_{Load}.f_{Sw} + K_{cond}.f_{Sw} + K_{gates}.f_{Sw} + K_{par}.f_{Sw} + K1_{Logic}.f_{Sw} + K2_{Logic}}$$

or

$$\eta(f_{Sw}) = \frac{K_{Load}}{K_{Load} + K_{cond} + K_{gates} + K_{par} + K1_{Logic} + \frac{K2_{Logic}}{f_{Sw}}} \tag{4.3}$$

From equation (4.3) it is clear that if the term $\frac{K2_{Logic}}{f_{Sw}}$ is negligible in comparison with the other terms of the denominator the efficiency is independent of the switching frequency. This assumption is valid for a wide range of the switching frequency. When the switching frequency is such that the previous assumption is not valid and the switching frequency continues decreasing the efficiency will start to degrade. On the other hand, if the switching frequency becomes high and the converter goes into the FSL mode, the output voltage will decrease when the load current becomes higher. Thus, the efficiency starts to decrease and will collapse.

Because of the above, the proposed feedback loop is the one shown in Figure 4.1. The difference voltage (V_d) between the output voltage (V_{OUT}) and a voltage reference (V_{REF}) is amplified with an operational amplifier. The output voltage of the amplifier is connected to the input of a Voltage Controlled Oscillator (VCO from now on). The output of the VCO is connected to the main clock of the converter. Thus, if the load current starts to increase, the output voltage will decrease. As a consequence V_d and the output of the amplifier will increase. Then the output frequency of the VCO will increase and the output voltage will increase, returning to the original value.

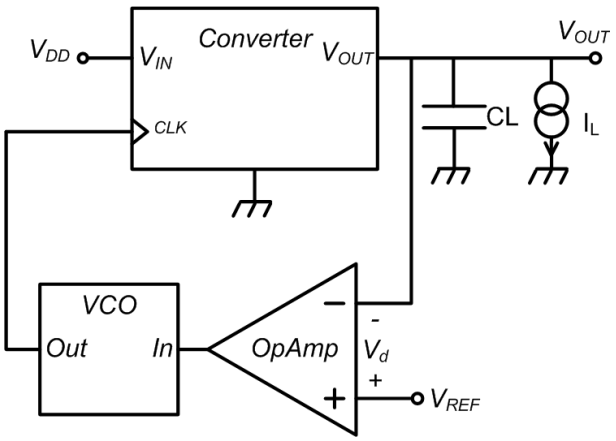


Figure 4.1: Proposed feedback loop.

4.2. V_{REF} Optimum Value

The efficiency of the converter has a strong dependence with the reference output voltage. For a given converter, load current, N and V_{REF} the switching frequency is given. If we increase V_{REF} the feedback loop is going to increase the frequency to decrease the difference voltage. So the conduction losses will decrease (less voltage drop in the output resistance) but the other losses will increase (larger switching frequency). On the other hand, if we decrease V_{REF} the feedback loop will decrease the switching frequency and effect in losses will be the opposite. So there is an optimum V_{REF}.

To calculate the optimum value of V_{REF} we must open the loop and make variations in the switching frequency. These variations will make variations in the output resistance and as consequence in the average output voltage. In a switching frequency f_{Sw}^{OPT} the output average voltage will be V_{OUT}^{OPT} and the efficiency will be maximum. If when we close the loop we use as a voltage reference the optimum output average voltage ($V_{REF} = V_{OUT}^{OPT}$) the feedback loop will adjust the switching frequency to f_{Sw}^{OPT} and the efficiency will be optimum. Figure 4.2 shows this analysis made with Matlab for the designed converter, a conversion ratio of $\frac{4}{5}$, $N = 8$ and $I_L = 50\mu A$. In the upper graphic it can be seen that the optimum value of V_{REF} in this case is $\simeq 2V$. In the bottom graphic the losses are shown as percentage of the total losses. This graphic shows how for the highest output voltages the frequency is too high and the logic, parasitic capacitances and gate drive losses are dominant. On the other hand, for the lowest output voltages the voltage drop in the output resistance is high and conduction losses are dominant.

4.3. About the Feedback Loop

Here it is important to highlight that the feedback loop as such can oscillate, have high overshoot or very long settling times. So to design the amplifier and the VCO a small signal model of the converter must be developed. The union amplifier-VCO does implement the controller, so the small signal model of the converter must be with the

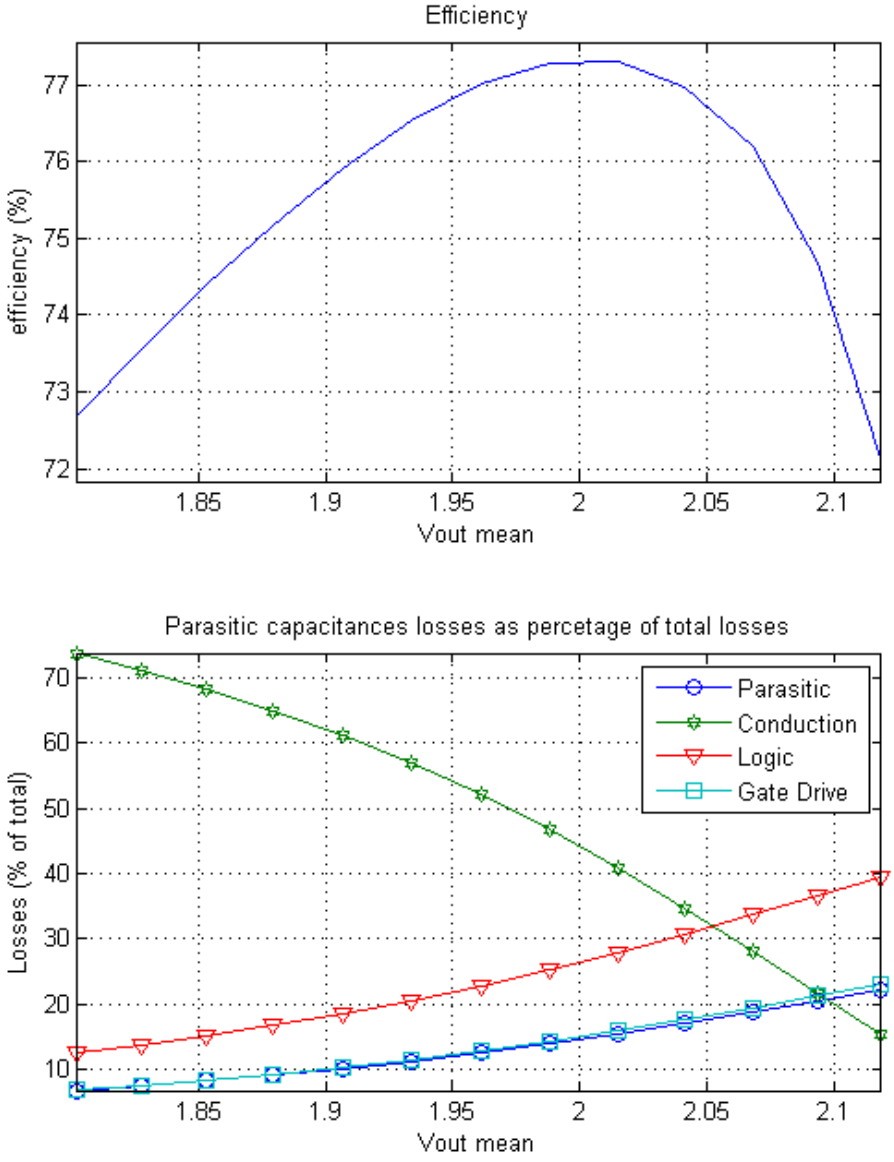


Figure 4.2: Optimum V_{REF} selection.

form:

$$V_{OUT} = H(s).f_{Sw} \tag{4.4}$$

Such a model is out of the scope of this thesis but should be obtained either by analysis or simulations in order to design the loop gain.

CHAPTER 5

Results and Comparison with Other Works

In this chapter the designed converter is presented. First, the dimensions of all the main components are shown. Then, a detailed analysis of the performance of the converter for the four conversion ratios is performed. At last, the global performance of the converter is presented and a comparison with existing works is made, in particular an analysis of the main differences.

5.1. Results

The presented converter was designed and simulated with the technology $On - Semi\ 0{,}5\mu m$. Table 5.1 shows the data converter designed with exception of buffers dimensions and logic. Then, Figure 5.1 shows the efficiency of the converter as a function of the load delivered power for the conversion ratios $2/5$ and $4/5$.

Figure 5.2 shows the performance of the converter for the conversion ratio $4/5$. A comparison between the performance with and without the parasitic losses reduction technique is performed. In the upper graphic the efficiency is shown and it can be seen that the value is significantly lower when the reduction technique is not applied. The explanation of this difference can be seen in the graphics where the losses are shown as percentage of total losses. In the case where the losses reduction technique is not applied the dominant losses are the parasitic capacitances losses. When the technique is applied the parasitic capacitances losses significantly decrease, and the dominant losses are the conduction losses. Gate driving losses are the less significant in all the current load range for both cases.

If we look at the efficiency in the case when the losses reduction technique is applied it is clear that it is approximately constant in the current load range $10 - 100\mu A$. This is a consequence of the switching frequency variaton proportionally to the current load (This dependence between current load and switching frequency was emulated because the feedback loop was not implemented).When the current load is in the range

Parameter	Unit	Value	Comment
w_{CL}	μm	2000	Width of the load capacitor C_L.
l_{CL}	μm	2000	Length of the load capacitor C_L.
C_L	nF	13	Load capacitor.
w_{CRing}	μm	1000	Width of the ring capacitors C_{Ring}.
l_{CRing}	μm	1000	Length of the ring capacitors C_{Ring}.
$CRing$	nF	3.25	Ring Capacitors (there are five of this one.)
$wn_{SWInter}$	μm	247	Width of the n transistor of the switch $SWInter$.
$wp_{SWInter}$	μm	619	Width of the p transistor of the switch $SWInter$.
wn_{SWT2}	μm	22.6	Width of the n transistor of the switch $SWT2$.
wp_{SWT2}	μm	56.4	Width of the p transistor of the switch $SWT2$.
wp_{SWT1}	μm	56.4	Width of the p transistor of the switch $SWT1$.
wn_{SWGnd}	μm	247	Width of the n transistor of the switch $SWGnd$.
f_{Sw}@100μA	MHz	1	Switching frequency.
I_{BIAS}	nA	100	Current that foresees the implementation of analog circuits.
n	$Unit$	5	Number of capacitors that implement the ring.
V_{DD}	V	2.8	Supply Voltage

Table 5.1: Designed converter parameters. Technology used $On - Semi$ 0,5μm

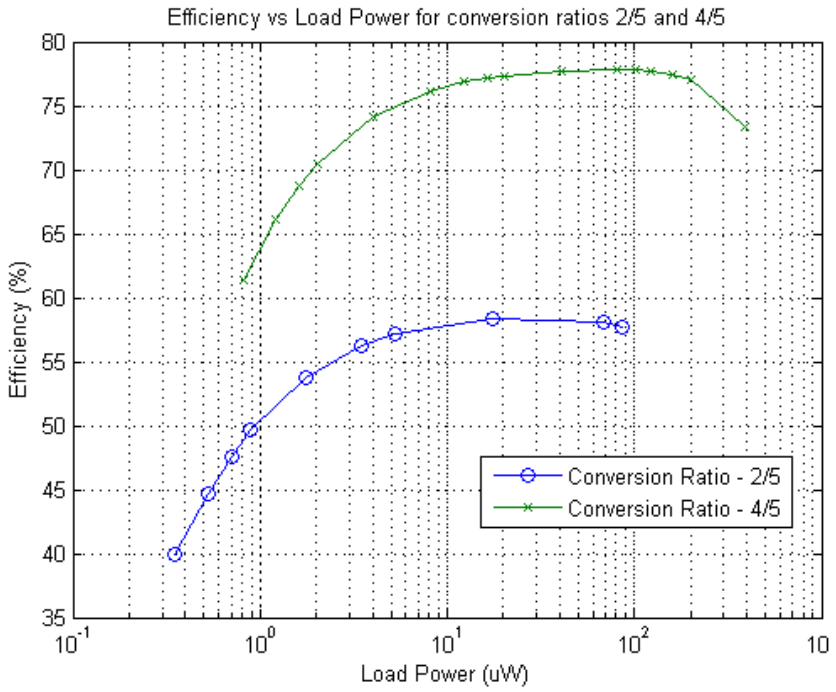


Figure 5.1: Efficiency vs load power.

$0{,}1 - 10\mu A$ the efficiency decreases because the constant term ($K2_{Logic}$) in the equation (4.3) becomes more significant[1]. This can be seen in the graphic where the losses are shown, where the logic losses come to be dominant in this range of currents. On the other hand, if we look at the efficiency for the highest current values (60, 80 and $100\mu A$) it is clear that it has a gentle downward trend. This is because the resistance of FSL mode (R_{FSL}) starts to be more significant and the mechanism described in the Chapter 4 to keep the drop voltage constant in the output resistance starts to be not effective.

Then, if we look the case of $I_L = 200\mu A$ it is clear that the output voltage and the efficiency have an abrupt reduction. This is because the operation mode of the converter is much near the FSL than for the case $I_L = 100\mu A$. Another interpretation that can be made for this behavior is in terms of voltage waveforms. While in the case of $I_L = 100\mu A$ the phases duration is enough to consider that the different capacitor voltages achieve the steady state ($T1 \simeq 3.\tau$), in the case $I_L = 200\mu A$ the frequency becomes twice with respect to the other case and the phases duration is not enough to achieve steady-state in capacitor voltages ($T1 \simeq 1{,}5.\tau$). As a consequence the output voltage decreases and the conduction losses too.

On the other hand, there is a similar situation in the case of the application of the parasitic capacitances losses reduction technique. Phases duration are too short and there is no time to redistribute the charge between the parasitic capacitances that needs to lose energy and the ones that need to gain it. So the parasitic capacitances losses increase too. In the graphic where the losses are shown these effects can be seen, where both type of losses have increased abruptly for this value of load current.

In the graphic where the average output voltage is shown it is clear that the mechanism to keep the output voltage constant works very well in the current range $400nA - 10\mu A$ so we can conclude that the output resistance is inversely proportional to the switching frequency and the converter is working in SSL mode. However, in the range $10 - 100\mu A$ the output voltage starts to decrease. As stated in the previous paragraph the resistance R_{FSL} starts to be more significant and the transition between SSL and FSL modes starts. Unlike the graph showing the efficiency which contains two curves, here only one curve is presented because applying the reduction losses technique has no effect on the output voltage.

Figures 5.3, 5.4 and 5.5 shows the performance of the converter for the conversion ratios of 3/5, 2/5 and 1/5 respectively. The situation is practically the same for all the cases with the exception of the fact that the lesser the conversion ratio is the lesser the efficiency for a given load current is. This is because for a lower conversion ratio the power delivered to the load is lower while the logic, parasitic capacitances and gate drive losses keeps equal.

5.2. Comparison with Other Works

Although some works about this topic in the literature exist, just [7] and [8] have very similar specifications with this work, so the comparison is made with these two.

[1] This term comes from the integration of the power of analog circuits such as amplifiers of comparators ($100nA$ in this case).

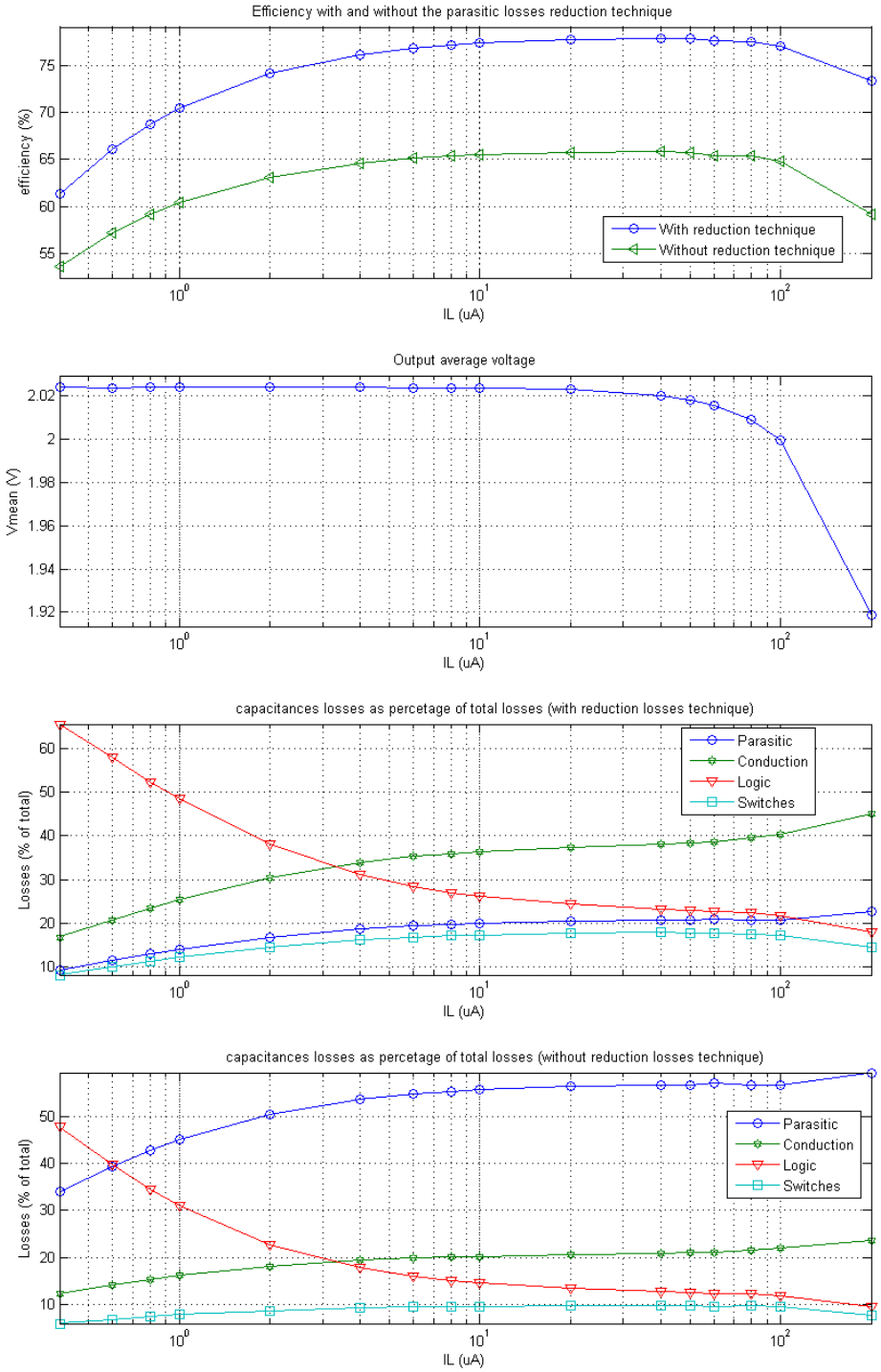


Figure 5.2: 4/5 conversion ratio performance.

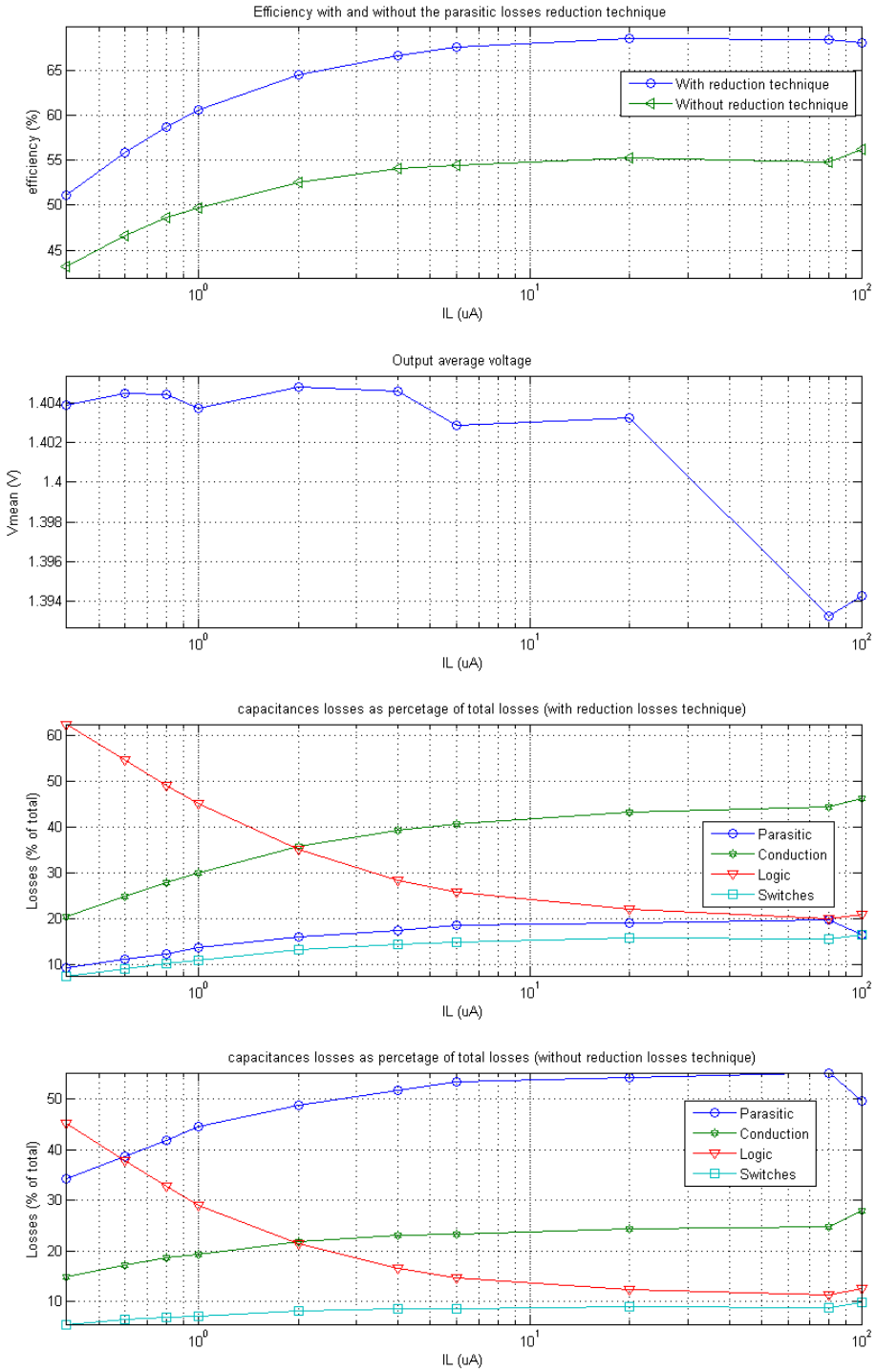


Figure 5.3: 3/5 conversion ratio performance.

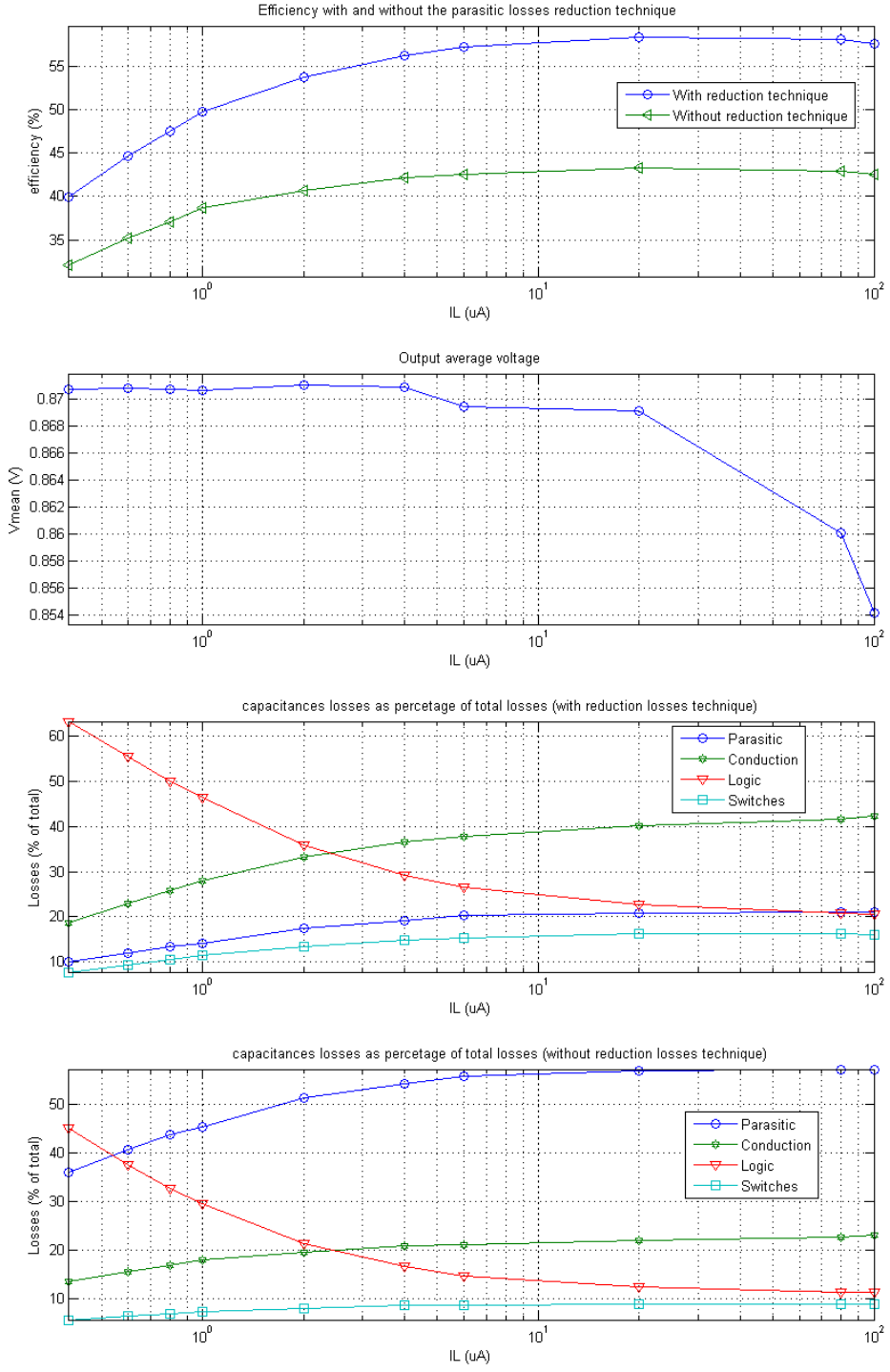


Figure 5.4: 2/5 conversion ratio performance.

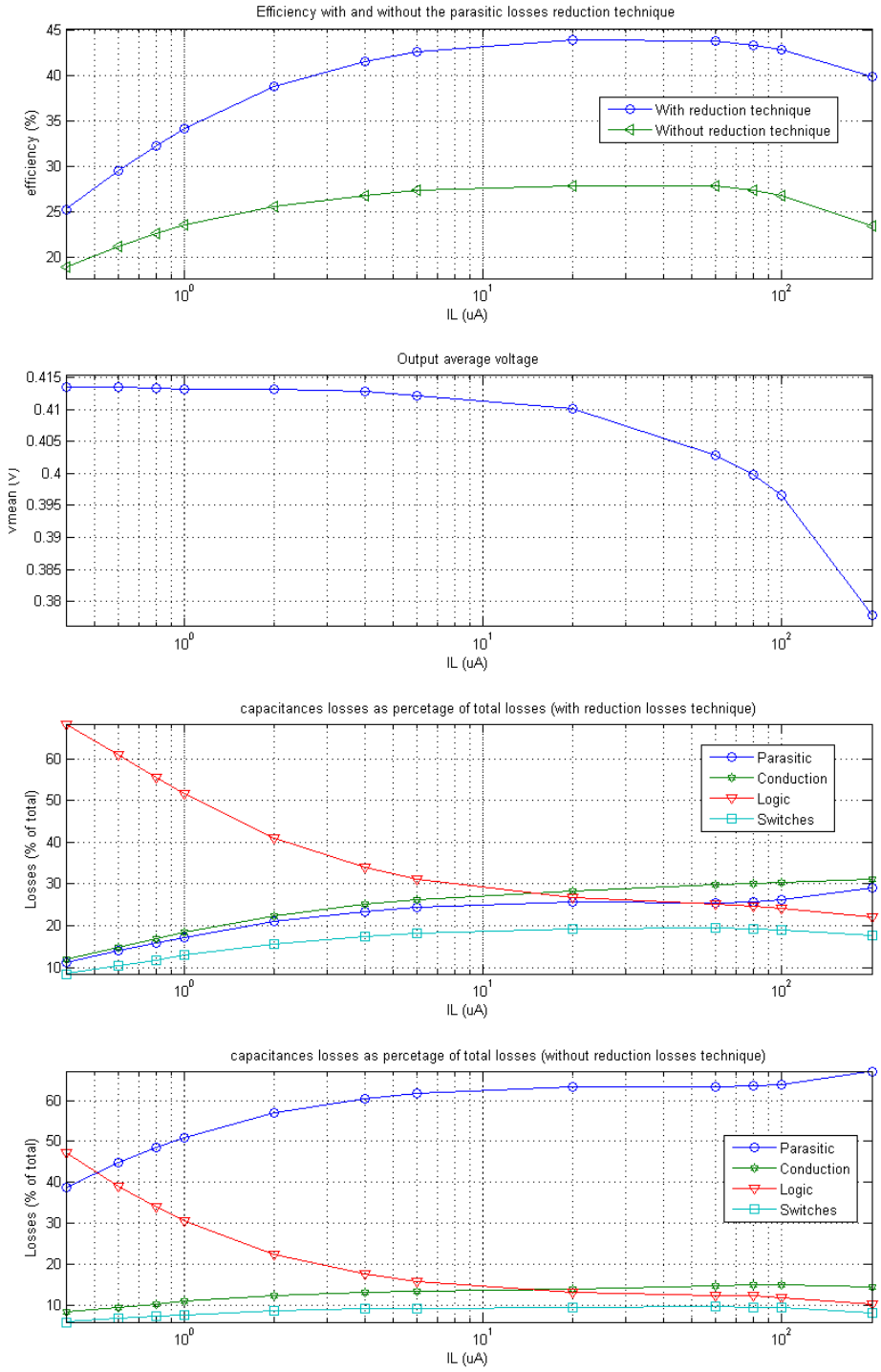


Figure 5.5: 1/5 conversion ratio performance.

Design	[8]	[7]	This work
Technology	0.13 μm	0.18 μm	0.5 μm
Chip Active area*	$0{,}52mm^2$	$0{,}57mm^2$	$10mm^2$
Total On-Chip Cap	$350pF$	$2{,}4nF$	$29nF$
Number or conversion ratios	3	5	5**
V_{OUT}	$1{,}1 - 0{,}3V$	$1{,}1 - 0{,}3V$	$0{,}4 - 2V$
V_{DD}	$1{,}2V$	$1{,}2V$	$2{,}8V$
Minimum load current	$1\mu A$	$10\mu A$	$1\mu A$
Load power range	$1 - 230\mu W$	$5\mu W - 1mW$	$0{,}5 - 200\mu W$
Efficiency range	$80 - 30\,\%$	$80 - 50\,\%$	$78 - 35\,\%$
Operating frequency	asynchronous	$15/7{,}5/3{,}75MHz$	$10kHz - 1MHz$

* Not included pads and interconnections.
** While in all the text a four conversion ratio converter is mentioned (1/5, 2/5, 3/5 and 4/5), the unit conversion ratio can be added to the converter without any impact.

Table 5.2: Comparison with other works.

Parameter	Unit	On Semi $0{,}5\mu m$	IBM $0{,}13\mu m$	IBM $0{,}18\mu m$
C_{ox}	aF/um^2	2356	10323	8275
V_{T0n}	V	0.8	0.42	0.46
V_{T0p}	V	-0.88	-0.42	-0.41

Parameters obtained from the web site of MOSIS organization from specific runs.

Table 5.3: Capacitance per unit area comparison.

Table 5.2 shows the general characteristic of the designed converter and makes the mentioned comparison.

The on-chip capacitor total value used in this work is much larger than the ones used by the two other works, this can be explained by two factors. The first one (and less important) is that the designed converter is not optimized and it is possible that making a local design space exploration around the current design point this value could be reduced. The other and most important factor is the technology used, the one used by the other works allows to work with a lower supply voltage (it will be explained next) with the impact that it has in digital circuit consumption (decreases quadratically with the supply voltage). Furthermore, it allows to have smaller switches because the resistance of a switch is inversely proportional to the Gate-Oxide capacitance, and as shown in the Table 5.3 these technologies have higher values. Summarizing implementing the converter with these technologies will allow to have an abrupt reduction in all the loss factors that are directly affected by the switching frequency, so it will allow to significantly increase this parameter. So, it is possible to reduce significantly the capacitor values without jeopardizing the output resistance value. In fact [7] uses a switching frequency in the range $15 - 3{,}75MHz$. So if for example we can use a maximum switching frequency of $10MHz$ instead $1MHz$ as used actually, the capacitor values can be reduced to $2{,}9nF$ keeping the same output resistance.

If we make a comparison in terms of area, the one used in this work is approxi-

Parameter	[7]	This Work
$Type of data$	Measured	Simulation
V_{OUT}/V_{DD}	0,667	0,714
$Load\ Power$	$100\mu W$	$100\mu W$
$Efficiency$	76,3 %	77,9 %
$Conduction\ Losses$	$12{,}45\mu W$	$11{,}1\mu W$
$Parasitic\ Losses$	$7{,}47\mu W$	$6\mu W$
$Gate\ drive\ Losses$	$6{,}38\mu W$	$5{,}15\mu W$
$Control\ Losses$	$4{,}69\mu W$	$6{,}67\mu W$

Table 5.4: Performance comparison in a particular situation.

mately twenty times larger than the one used by the other works. Taking into account that the area is in general dominated by capacitors in this type of circuits, this big difference again can be explained in terms of technology differences. First of all, because the capacitors used in this work are based on PMOS capacitors and the Gate-Oxide capacitance per unit area is approximately four times larger for the others technologies, simply changing the technology will allow to reduce the area to one quarter. This reduction is made keeping the same total capacitor value. In addition, because what is mentioned in the previous paragraph this change of technology would allow to reduce significatively the total capacitor value. If this reduction could be made in the order of five times smaller, the total area of capacitors will be reduced twenty times that is the above mentioned difference.

The other parameters have similar values with exception of supply voltage and switching frequency. The switching frequency was analyzed previously so we will discuss the difference in supply voltage. The main reason of this difference is due to the different threshold voltage (V_{T0}) of the technologies. This parameter puts a low limit to the supply voltage given by the equation (5.1) ([15]) where V_{T0n} and V_{T0p} are the threshold voltage for transistors n and p respectively, and n_n and n_p are the subthreshold slope factor of the transistor n and p respectively. The objective of this minimum limit is to avoid the gap that can exist in the conduction of the switch if there is a strip where none of the two transistors are conducting. The values of V_{T0} are shown in Table 5.3 where it can be seen that the $On - Semi 0{,}5\mu m$ technology has a larger value in both types of transistors. As mentioned, the supply voltage has a quadratic direct impact in the logic consumption so the difference in this parameter of the technology (V_{T0}) has a very important impact.

$$V_{DD}^{Min} = \frac{n_n.V_{T0p} + n_p.V_{T0n}}{n_n + n_p - n_n.n_p} \tag{5.1}$$

At last, in a particular situation a comparison with [7] is performed. Table 5.4 shows this comparison, where it can be seen that for a very similar situation (almost equal conversion ratio and equal load power) not only the efficiency has a very similar value, but the four types of losses have very similar values.

CHAPTER 6

Conclusions and Future Work

A novel architecture for a **Ultra Low Power Switched Capacitor DC-DC Converter** was proposed. This architecture is modular (each module was named as **Basic Capacitor Cell**) and allows to add easily new conversion ratios if needed. An example of a **Switched Capacitor Converter** with five **Basic Capacitor Cells** was implemented and electrically simulated. This simulation was made for the four conversion ratios and for currents from $400nA$ to $100\mu A$. The efficiency achieved is above $77\,\%$ for one order of magnitude of the current load for the conversion ratio $4/5$. The efficiency achieved is comparable with the existing works in the literature mainly [7] and [8].

A feedback loop mechanism was proposed. It consist in changing the switching frequency proportionally to the current load. It allows to have just the needed switching (in logic and switches) having a constant efficiency in a wide range of load currents. The proposed control is built regulating the output voltage with an operational amplifier and a VCO (Voltage Controlled Oscillator). The frequency of the waveform provided by the VCO, which is proportional to the load current, is connected to the main clock of the converter. Because the feedback loop was not implemented it was emulated in the electrical simulations. The result was a set of curves of efficiency that has a planar behavior in a wide range of currents for all the conversion ratios.

As parasitic capacitances losses are dominant, a novel technique to reduce these losses was implemented. This technique results in an improvement approximately of $10\,\%$ in the efficiency from a $80\,\%$ reduction in the mentioned losses.

A generical numerical model was developed that is useful to make design space exploration. As the architecture is modular and the model uses some electrical parameters extracted from electrical simulations and parameters of the technology, it is easy to adapt the model for other technologies.

Although the comparison with the existing works in the literature has as result that a similar performance is reached, a much larger total capacitor value and a larger area

were used. This difference is explained in terms of the used technology. A first order analysis was made, showing that both differences can be significantly reduced just implementing the converter in more modern technology.

6.1. Future Work

Although the general performance of the converter is very similar to the one of existing works, it was paying a significative price in area and total capacitance, making it difficult to compare. To have a more realistic comparison, implementing a converter using the proposed architecture in a more appropriate technology is central.

The logic was implemented but not optimized. As shown for example in Figure 5.2 for low currents the losses in the logic are dominant, so making an optimization in this part of the circuit can achieve an increase in the general efficiency and a decrease in the minimum load current.

The designed converter was achieved from electrical simulations, analyzing the different losses and changing parameters to improve them. So it is not sure that the design point chosen is the better. A design space exploration must be made to analyze if a better design exists.

As mentioned in Chapter 4 a small signal-model must be developed for the converter in order to make a design of the controller that ensures the stability of the feedback loop.

If the feedback loop is implemented, when the load current decreases the switching frequency decreases too, but the different components of the converter (switches and capacitors) remain the same, in particular the time constants (τ) of the different phases remain equal. But if the switching frequency is reducing the time constants can be increased too without jeopardizing the average output voltage and the efficiency of the converter. The increase in τ can be implemented increasing the capacitors or the switches resistances. As increasing capacitors affects the output resistance it is better to make a reduction in the switches width. This allows to improve the efficiency due to a decrease in the gate drive losses. [8] uses a similar mechanism subtracting or adding switches in parallel as needed.

At last, future work should also include fabricating and testing the converter.

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APPENDIX A

Numerical Model Data Construction

This appendix describes the different user defined functions used in the numerical model in Matlab. Figure A.1 shows the files used tree.

A.1. File Tree

This section describes each defined function and the data that the user must introduce. The explanation of each input and output of the different functions is made in each file.

A.1.1. FunctionPerformanceFinal.m

This is the main function that calculates the performance of the converter. It calculates the charge in all the capacitors as function of time and the different energies involved as energy delivered to the load, parasitic capacitances lost energy, etc. From this data it calculates the efficiency and output voltage waveform. How this function works it is described in Section 3.5.

Technology Necessary Data

It is not necessary to introduce technology data in this file because all the data needed is taken by the file amis05um.m.

A.1.2. amis05um.m

This file have the objective of concentrate some technology data used by the model.

Technology Necessary Data

- Wnmin [μm] - Minimum width of n transistor.
- Wpmin [μm] - Minimum width of p transistor.

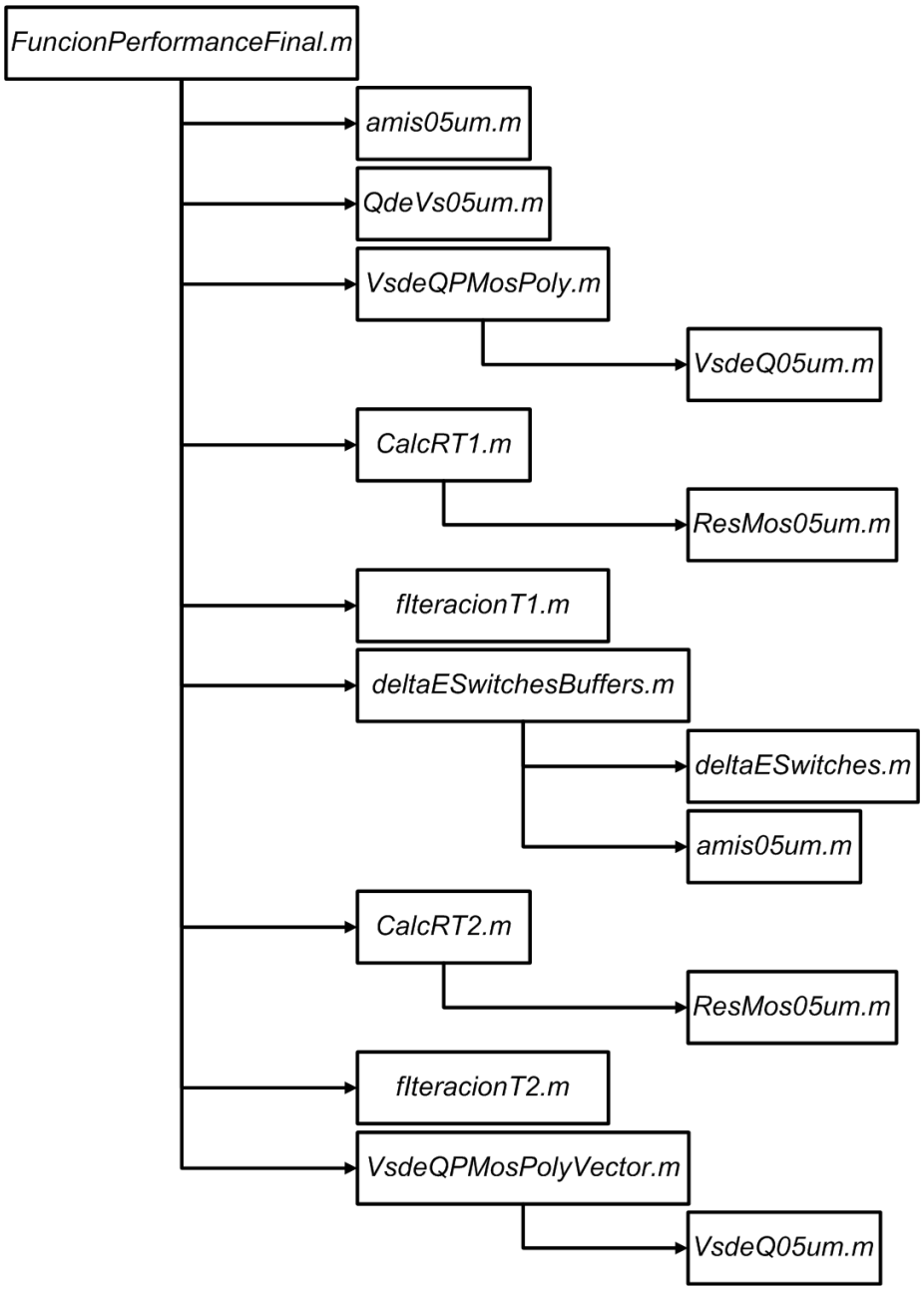

Figure A.1: Files Tree

- DeltaEInverter [$Jouls/\mu m$] - Energy per width unit consumed in a On-Off cycle of an inverter. This data must be extracted from electrical simulation. It is very important that it takes into account the fun-out used in the drivers of the switches. If for example all the inverters have as load another inverter four times widther this must be taken into account in the simulation used to extract the data.
- DeltaELogicT1T2 [Jouls] - Energy consumed by the logic in each process of on-off of the both switches $SWT1$ y $SWT1$.
- DeltaELogicRot [Jouls] - Energy consumed by the logic in each process of rotation of the ring.
- CnArea [$F/\mu m^2$] - Parasitic capacitance per area unit of the drain/source of n transistors.
- CnPer [$F/\mu m$] - Parasitic capacitance per length(perimeter) unit of the drain/source of n transistors.
- CpArea [$F/\mu m^2$] - Parasitic capacitance per area unit of the drain/source of p transistors.
- CpPer [$F/\mu m$] - Parasitic capacitance per length(perimeter) unit of the drain/source of p transistors.
- LDSn [μm] - Length of the drain/source area of n transistors.
- LDSp [μm] - Length of the drain/source area of p transistors.
- CPolyArea [$F/\mu m^2$] - Capacitance per area unit of ploy1-poly2 capacitors.
- CPolyPer [$F/\mu m$] - Capacitance per length(perimeter) unit of ploy1-poly2 capacitors.
- CNWellSust [$F/\mu m^2$] - Parasitic capacitance per area unit of the NWell-Substrate diode.

A.1.3. QdeVs05um.m

This function calculates the charge of a PMOS capacitor as a function of the bias voltage and his length and width.

Technology Necessary Data

This function uses a two rows matrix ("f" in the .m file), the data is extracted from electrical simulation. The electrical simulation must be made with large capacitors ($1000 * 1000 \mu m^2$ for example). The numerical simulation do not take into account the effective length or width so minimal transistors must be avoided.

- Capacitor Voltage [V] (First row) - Voltage between plates of the capacitor.
- Charge [$Coulomb/\mu m^2$] (Second row) - Charge per area unit.

A.1.4. VsdeQPMosPoly.m

This function returns the voltage of a capacitor composed by a poly1-poly2 and a PMOS capacitor.

Technology Necessary Data

- CPolyArea $[F/\mu m^2]$ - Capacitance per area unit of ploy1-poly2 capacitors.
- CPolyPer $[F/\mu m]$ - Capacitance per length(perimeter) unit of ploy1-poly2 capacitors.

A.1.5. VsdeQ05um.m

Implements the inverse function of **QdeVs05um.m**.

Technology Necessary Data

The data needed is the same that the function **QdeVs05um.m** needs, but the rows of the matrix must be interchanged.

A.1.6. CalcRT1.m

This function calculates the equivalent resistance for the phase $T1$ described in the equation 3.10

Technology Necessary Data

It is not necessary to introduce technology data in this file.

A.1.7. ResMos05um.m

This function calculates the resistance of a single switch (one transistor). To calculate the resistance of a composed switch it is necessary to call the function two times and calculate the parallel equivalent.

Technology Necessary Data

The necessary data for this function is the resistance per width unit for n and for p transistors. It uses a three rows matrix (named "f1" in the file), the data of the matrix is extracted from electrical simulations.

- Source Voltage $[V]$ (First row) - Source bias voltage.
- n resistance $[\Omega.\mu m]$(Second row) - n transistors resistance per unit width.
- p resistance $[\Omega.\mu m]$(Third row) - p transistors resistance per unit width.

It is important to notice that these data is extracted for a given supply voltage (V_{DD}). To makes a numerical simulation with other value of V_{DD}, an electrical simulation must be made and the data introduced in the matrix "f1" again.

A.1.8. fIteracionT1.m

This function implements the equation 3.13

Technology Necessary Data

It is not necessary to introduce technology data in this file.

A.1.9. deltaESwitchesBuffers.m

This function calculates the switches consumption including the buffers consumption. Although no technology data is needed in this file, two design criteria must be included. The first one is the fun-out ("funout" in the .m file) of the inverters that must be equal for all them. The second one is the ratio between the width of the n and p transistors ("wpsobrewn" in the .m file) in the different inverters. If for example the inverters where designed having the p transistor witdh two times larger than the one of the n transistor this parameter must be 2.

Technology Necessary Data

It is not necessary to introduce technology data in this file.

A.1.10. deltaESwitches.m

This function calculates the consumption of driving the gates of the switch transistors not including the buffers consumption.

Technology Necessary Data

It uses a three row matrix (named "f" in the .m file), the matrix data is extracted from electrical simulations.

- Source Voltage $[V]$ (First row) - Source bias voltage.
- n transistor gate drive consumption $[Jouls/\mu m]$(Second row) - Consumption per width unit of driving the n transistor gate.
- p transistor gate drive consumption $[Jouls/\mu m]$(Third row) - Consumption per width unit of driving the p transistor gate.

It is important to notice that these data is extracted for a given supply voltage (V_{DD}). To makes a numerical simulation with other value of V_{DD}, an electrical simulation must be made and the data introduced in the matrix "f1" again.

A.1.11. CalcRT2.m

This function calculates the equivalent resistance for the phase $T2$ described in the equation 3.18

Technology Necessary Data

It is not necessary to introduce technology data in this file.

A.1.12. fIteracionT2.m

This function implements the equation 3.23

Technology Necessary Data

It is not necessary to introduce technology data in this file.

A.1.13. VsdeQPMosPolyVector.m

It is used to calculate the voltage as a function of the time from a vector that contains the charge as a function of the time.

Technology Necessary Data

- CPolyArea [$F/\mu m^2$] - Capacitance per area unit of ploy1-poly2 capacitors.
- CPolyPer [$F/\mu m$] - Capacitance per length(perimeter) unit of ploy1-poly2 capacitors.

APPENDIX B

Energy Transference Between Capacitors

To calculate the energy delivered from capacitor $C1$ to capacitor $C2$ (look Figure B.1) we have that the initial conditions are the following:

$$\left.\begin{array}{c} V1_i = V_i \\ V2_i = V_i - \Delta V \\ and \\ Q1_i = C1.V_i \\ Q2_i = C2.(V_i - \Delta V) \end{array}\right\} Initial \quad Conditions \tag{B.1}$$

To calculate the efficiency of the energy transfer we calculate the initial energy in the system, and the initial energy in the capacitor $C2$.

$$E2_i = \frac{C2}{2}.(V_i - \Delta V)^2 \tag{B.2}$$

$$Ei = E1_i + E2_i = \frac{C1}{2}.V_i^2 + \frac{C2}{2}.(V_i - \Delta V)^2$$

$$= \frac{C1 + C2}{2}.V_i^2 + \frac{C2}{2}.(\Delta V)^2 - C2.V_i.\Delta V \tag{B.3}$$

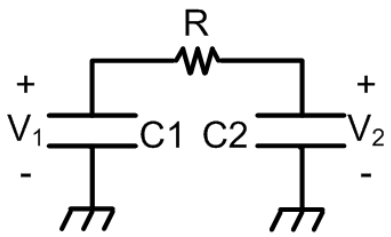

Figure B.1: Capacitor to capacitor charge transfer.

As the final state is when the voltage is the same in $C1$ and $C2$ we have that:

$$V1_f = V2_f = V_f = \frac{Q1_f}{C1} = \frac{Q2_f}{C2} \Rightarrow Q2_f = \frac{C2}{C1}.Q1_f \tag{B.4}$$

And the charge in the system is the same:

$$Q1_f + Q2_f = Q1_i + Q2_i \tag{B.5}$$

So from (B.1), (B.4) and (B.5):

$$Q1_f = (C1.V_i + C2.(V_i - \Delta V)).\left(\frac{C1}{C1+C2}\right) \tag{B.6}$$

And the final voltage in both capacitors is:

$$V_f = \frac{Q1_f}{C1} = (C1.V_i + C2.(V_i - \Delta V)).\left(\frac{1}{C1+C2}\right) = V_i - \frac{C2}{C1+C2}.\Delta V \tag{B.7}$$

Then, the final stored energy in the system is:

$$E_f = E1_f + E2_f = \frac{C1}{2}.V_f^2 + \frac{C2}{2}.V_f^2 = \frac{C1+C2}{2}.V_f^2$$

$$E_f = \frac{C1+C2}{2}.\left(V_i - \frac{C2}{C1+C2}.\Delta V\right)^2$$

$$E_f = \frac{C1+C2}{2}.\left(V_i^2 - 2.\frac{C2}{C1+C2}.V_i.\Delta V + \left(\frac{C2}{C1+C2}.\Delta V\right)^2\right)$$

$$E_f = \frac{C1+C2}{2}.V_i^2 - C2.V_i.\Delta V + \frac{(C2.\Delta V)^2}{2.(C1+C2)} \tag{B.8}$$

To calculate the energy dissipated[1] in the process we have from equations (B.3) and (B.8) that:

$$\boxed{\boxed{E_{Lost} = \Delta E = E_f - E_i = -\frac{C1.C2.\Delta V^2}{2.(C1+C2)}}} \tag{B.9}$$

Then, the final energy in capacitor $C2$ is:

$$\Delta E2_f = \frac{C2}{2}.V_f^2 \tag{B.10}$$

So from equations (B.2), (B.7) and (B.10):

$$\boxed{\boxed{\Delta E2 = \frac{C1.C2}{C1+C2}.\left(V_i.\Delta V - \frac{\Delta V^2}{2}.\left(\frac{C1+2.C2}{C1+C2}\right)\right)}} \tag{B.11}$$

To calculate the efficiency of delivering energy from $C1$ to $C2$ we have the following equation:

[1] This energy is dissipated in the resistor R (Figure 1.2)

$$\boxed{\eta = \frac{\Delta E2}{\Delta E2 + E_{Lost}}} \tag{B.12}$$

And from equations (B.9) and (B.11) it can be seen that if $\Delta V \rightarrow 0$ the energy dissipated decreases faster than the energy delivered to $C2$ so $\eta \rightarrow 1$.